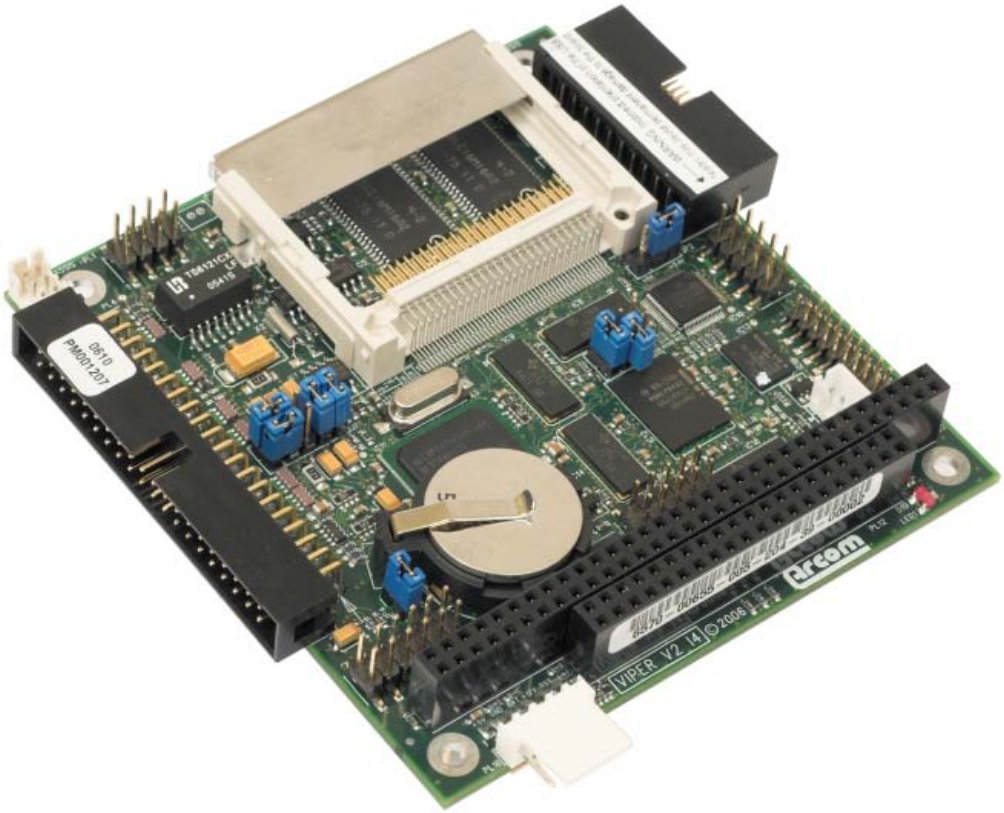
VIPER / VIPER-Lite

PXA255 RISC based PC/104 Single Board Computer

Technical Manual



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Revision History

Manual	*PCB*	*Date*	*Comments*
Issue A	V2 Issue 3	29th June 2005	First full release of Manual for VIPER Version 2.
Issue B	V2 Issue 4A	9th August 2006	Updated to include VIPER-Lite details, support for Intel P30 Flash, and for full RoHS-6 compliance.
Issue C	V2 Issue 4A	25th January 2007	Updated to show USB cables with Type A Plugs used to connect to USB Host and Client connectors PL7 and PL17 respectively.
Issue D	V2 Issue 4A	25th April 2007	Updated to show RS422/485 termination resistor jumpers disconnected as default

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Contents

Introduction 4
VIPER ‘at a glance’ 5
VIPER-Lite ‘at a glance’ 6
VIPER features 7
VIPER support products 9
Product handling and environmental compliance 12
Conventions 13
Getting started 15
Using the VIPER 15
Detailed hardware description 18
VIPER block diagram 18
VIPER address map 19
Translations made by the MMU 20
PXA255 processor 21
PXA255 GPIO pin assignments 22
Real time clock 26
Watchdog timer 26
Memory 27
Interrupt assignments 30
Flat panel display support 34
Audio 56
General purpose I/O 57
USB host interface 60
USB client interface 61
10/100BaseTX Ethernet 62
Serial COMs ports 64
PC/104 interface 67
I^2C 71
TPM 71
JTAG and debug access 72
Power and power management 73
Power supplies 73
Power management 74
Connectors, LEDs, and jumpers 85
Connectors 86
Status LEDs 97
Jumpers 98
Appendix A – Contacting Arcom 101
Appendix B – Specification 102
Appendix C – Mechanical diagram 103
Appendix D – Reference information 104
Appendix E – Acronyms and abbreviations 106
Appendix F – RoHS-6 Compliance - Materials Declaration Form 108
Index 109

Introduction

The VIPER is an ultra low power, PC/104 compatible, single board computer available in two standard variants:

- VIPER, based on the 400MHz PXA255 XScale processor.
- VIPER-Lite, based on the 200MHz PXA255 XScale processor.

The PXA255 is an implementation of the Intel XScale micro architecture combined with a comprehensive set of integrated peripherals including: a flat panel graphics controller, interrupt controller, real time clock, and multiple serial ports. The VIPER board offers a wide range of features making it ideal for power sensitive embedded communications and multimedia applications.

Both of the standard variants are available in two memory configurations, as shown below:

Variant	Memory configuration	Details
VIPER	VIPER-M64-F32-V2-R6	PXA255 400MHz microprocessor, 64MB SDRAM, 32MB FLASH.
	VIPER-M64-F16-V2-R6	PXA255 400MHz microprocessor, 64MB SDRAM, 16MB FLASH.
VIPER-Lite	VIPERL-M64-F32-V2-R6	PXA255 200MHz microprocessor, 64MB SDRAM, 32MB FLASH, with reduced functionality.
	VIPERL-M64-F16-V2-R6	PXA255 200MHz microprocessor, 64MB SDRAM, 16MB FLASH, with reduced functionality.

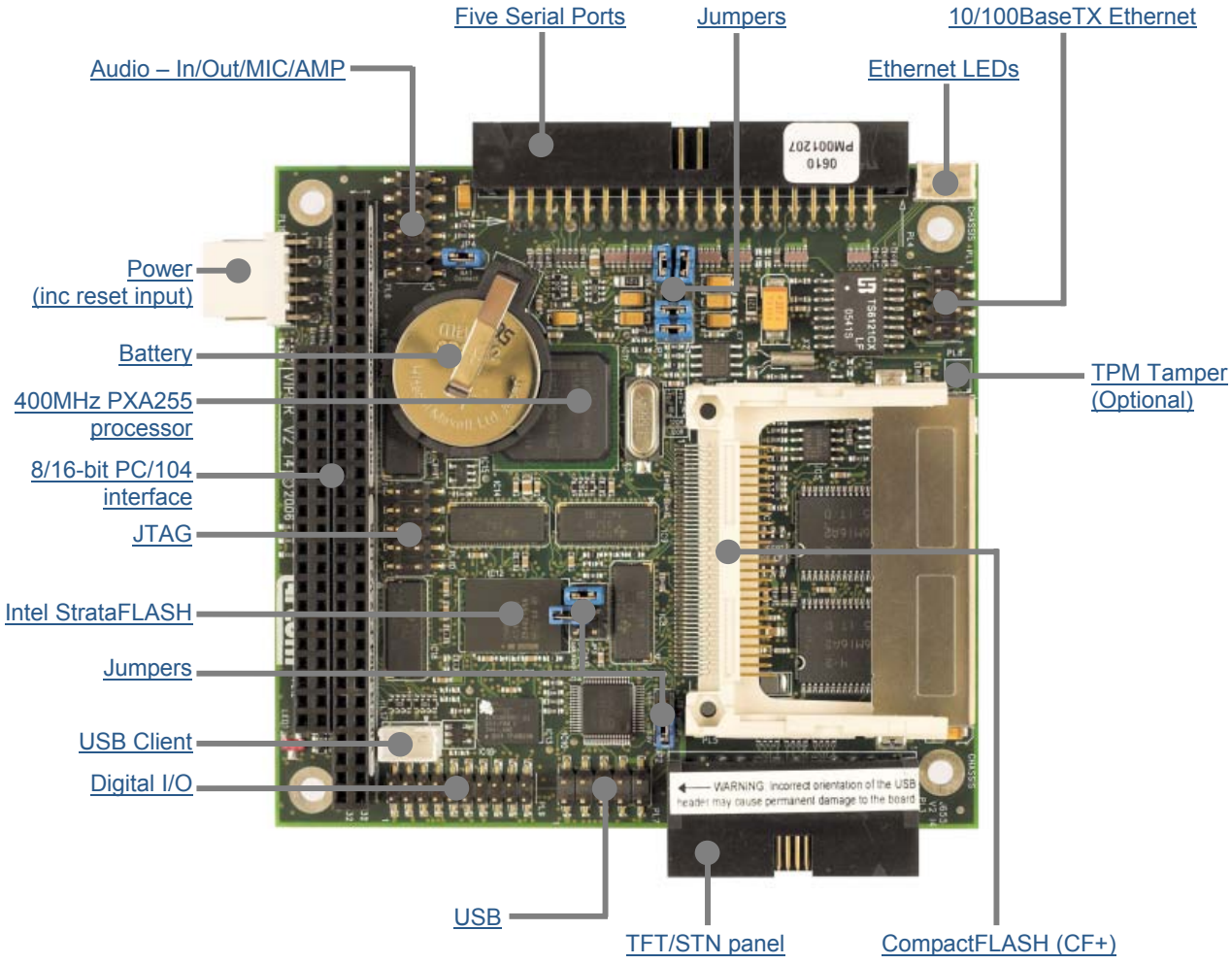
The VIPER and VIPER-Lite variants are also available in an industrial temperature range. Please contact our Sales team (see Appendix A – Contacting Arcom, page 101) for availability.

The following features are *not* available on the standard VIPER-Lite configuration:

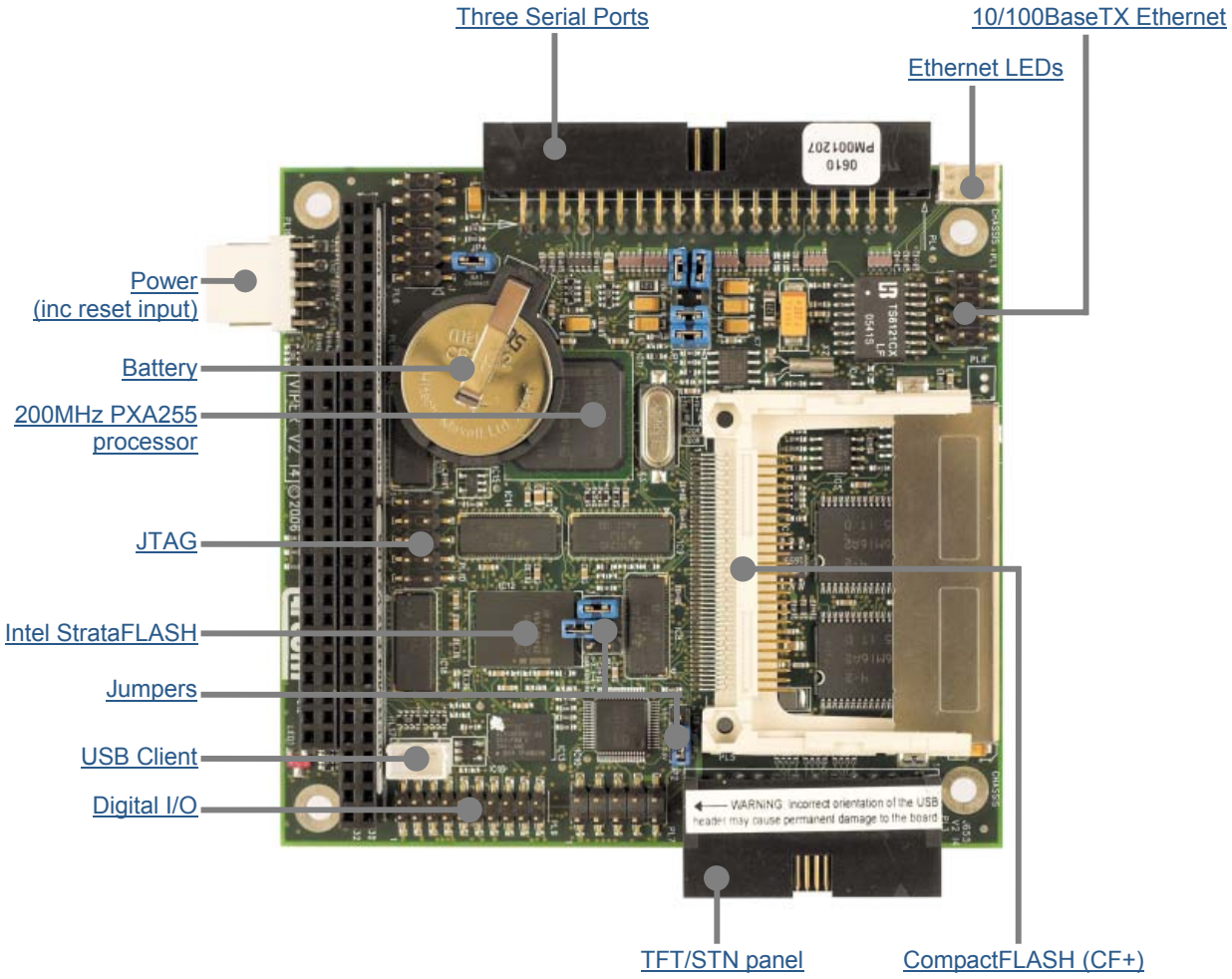
- PC/104 bus.
- USB host controller.
- Audio codec.
- COM4, COM5 serial ports.
- TPM (trusted platform module).
- SRAM (static random access memory).

Arcom can provide custom configurations (subject to a minimum order quantity) for the VIPER or the VIPER-Lite. Please contact our Sales team (see Appendix A – Contacting Arcom, page 101) to discuss your requirements.

VIPER ‘at a glance’



VIPER-Lite ‘at a glance’



VIPER features

Microprocessor

- PXA255 400MHz (VIPER) or 200MHz (VIPER-Lite) RISC processor.

Cache

- 32K data cache, 32K instruction cache, 2K mini data cache.

System memory

- 64MB un-buffered 3.3V SDRAM.

Silicon disk

- Up to 16/32MB Intel StrataFLASH (with FLASH access LED).
- 1MB bootloader FLASH EPROM (with FLASH access LED).
- ~~VL~~ 256KB SRAM (battery backed).
- Type I/II CompactFLASH (CF+) socket.

Video

- TFT/STN (3.3V or 5V) flat panel graphics controller.
- Up to 640X480 resolution.
- 8/16bpp.
- Backlight control.

Audio

- ~~VL~~ National Semiconductor LM4529 AC'97 CODEC and LM4880 power amp.
- ~~VL~~ Line IN, line OUT, microphone, and 250mW per channel amplified output.

Serial ports[1]

- 5 x 16550 compatible high-speed UARTs.
- 4 x RS232 and 1 x RS422/485 Interfaces.
- 2 x channels with 128Byte Tx/Rx FIFO.

USB host interface

- ~~VL~~ Two USB 1.1 compliant interfaces.
- Short circuit protection and 500mA current limit protection.

USB client interface

- One USB 1.1 client interface.

[1] COM4 (RS232) and COM5 (RS422/485) are not available on the VIPER-Lite.

Network support

- SMSC LAN91C111 10/100BaseTX Ethernet controller.
- One 10/100BaseTX NIC port.

Trusted Platform Module (TPM) [optional]

- VL Atmel AT97SC3201 TPM security, with full TCG/TCPA V1.1b compatibility.
- VL Includes crypto accelerator capable of computing a 1024-bit RSA signature in 100ms.

Real time clock (RTC)

- Battery backed RTC.
- ± 1minute/month accuracy, at 25°C.

Watchdog

- Adjustable timeout of 271ns to 19 minutes 25 seconds.

General purpose I/O (GPIO)

- 8 x 3.3V tolerant inputs (5V tolerant).
- 8 x 3.3V outputs.

User configuration

- 1 user-configurable jumper.

Expansion

- VL PC/104 expansion bus - 8/16-bit ISA bus compatible interface.

JTAG port

- Download data to FLASH memory.
- Debug and connection to In-Circuit Emulator (ICE).

Power

- Typically 2W from a single 5V supply.
- Power management features allowing current requirements to be as low as 49mA (245mW).

Battery backup

- Onboard battery holder containing a lithium-ion non-rechargeable CR2032, 3V, 220mAh battery.

Size

- PC/104 compatible footprint 3.8” x 3.6” (96mm x 91mm).

Environmental

- Operating temperature range:
  - Commercial: -20°C (-4°F) to +70°C (+158°F)
  - Industrial: -40°C (-40°F) to +85°C (+185°F)
- RoHS directive (2002/95/EC) compliant

VIPER support products

The VIPER supports the following products:

- **VIPER-UPS (Uninterruptible Power Supply)**
  The VIPER-UPS serves as a 5V DC power supply and battery back up system for the VIPER. The UPS accepts between 10 – 36 VDC (10-25VAC) input and generates the +5V supply for the VIPER. In addition to this, it includes an intelligent battery charger/switch capable of using either the onboard 500mAHr NiMH battery or an external sealed lead acid rechargeable battery. For further details, see www.arcom.com/products/icp/pc104/processors/viper_UPS.htm.

- **VIPER-FPIF1 (Flat Panel Interface)**
  The VIPER-FPIF1 is a simple board that enables easy connection between the VIPER and an LCD flat panel. See the section VIPER-FPIF1 details, page 38, for further details. Contact Arcom (see Appendix A – Contacting Arcom, page 101) for purchasing information.

- **ETHER-BREAKOUT**
  The ETHER-BREAKOUT is a simple board that converts the VIPER Ethernet 8-pin header and Ethernet LEDs 6-pin header to a standard RJ45 connector with LEDs. Contact Arcom (see Appendix A – Contacting Arcom, page 101) for purchasing information.

- **FPIF-LVDS-TX (Flat Panel Interface)**
  The FPIF-LVDS-TX enables LVDS displays to be connected to the VIPER. The FPIF-LVDS-TX in combination with the FPIF-LVDS-RX allows the VIPER to drive a TFT or STN LCD flat panel display up to 10 meters away. See the section FPIF-LVDS-TX details, page 43, for further details. Contact Arcom (see Appendix A – Contacting Arcom, page 101) for purchasing information.

- **FPIF-LVDS-RX (Flat Panel Interface)**
  The FPIF-LVDS-RX in combination with the FPIF-LVDS-TX allows the VIPER to drive a TFT or STN LCD flat panel display up to 10 meters away. See the section FPIF-LVDS-RX details, page 48, for further details. Contact Arcom (see Appendix A – Contacting Arcom, page 101) for purchasing information.

- **FPIF-CRT (CRT Monitor or Analog FPD Interface)**
  The FPIF-CRT is a simple board that enables easy connection between the VIPER and a CRT Monitor or analog LCD flat panel. See the section FPIF-CRT details, page 53, for further details. Contact Arcom (see Appendix A – Contacting Arcom, page 101) for purchasing information.

- **VIPER-I/O**
  VIPER-I/O is a low cost add-on I/O module for the PXA255 VIPER board. The board provides a variety of I/O features without the additional costs of a full PC/104 interface. The combination of the VIPER and VIPER–I/O is suited to control and monitoring applications that require a limited number of isolated inputs and outputs. See the section VIPER-I/O, page 59, for further details. Contact Arcom (see Appendix A – Contacting Arcom, page 101) for purchasing information.

- **CYCLOPS**
  The CYCLOPS is a rugged VIPER display terminal. The enclosure can be configured to suit a complete range of embedded applications with LCD display and touchscreen.

- **VIPER-ICE (Industrial Compact Enclosure) development kits**
  The VIPER-ICE is a simple low cost aluminum enclosure, which provides easy connection to all on board features. The enclosure includes the VIPER-UPS and optionally a color Q-VGA (320x240) TFT flat panel display and analog touchscreen. The VIPER-ICE is available with a wide range of development kits. These are described in the section Development kits available for the VIPER, page 10. For further details, see www.arcom.com/development-kits.htm.

Development kits available for the VIPER

- **Windows CE/CE 5.0 development kit**
  Features of this kit are:
  - 400MHz PXA255 processor with 64MB DRAM & 32MB Flash memory.
  - Pre-configured build of Windows CE 5.0 tailored specifically for the VIPER, pre-loaded into the 32MB Flash.
  - Windows CE 5.0 Platform SDK for VIPER.
  - Rugged enclosure with NEC Q-VGA TFT color 5.5 and display and analog touchscreen.
  - Uninterruptible power supply (VIPER-UPS) to allow VIPER system to continue to operate without main power. Example code is supplied to handle the power loss warning and battery backup control features.
  - 24V power supply module with power cords for US, UK, and European power sockets.
  - Arcom Development Kit CD containing Windows CE 5.0 operating system image, sample code, Technical Manual, and datasheets.
  - Quickstart manual.

- **Embedded Linux development kit**
  Features of this kit are:
  - 400MHz PXA255 processor with 64MB DRAM & 32MB Flash memory.
  - Pre-configured build of Arcom's Embedded Linux, tailored specifically for the VIPER, pre-loaded into the 32MB Flash.
  - 2.6-based Linux kernel release, GNU C library.
  - Compressed Journaling Flash File System (JFFS2) offering high reliability and recovery from power interruptions.
  - Rugged enclosure with optional NEC Q-VGA TFT color display and analog touchscreen.
  - Uninterruptible power supply (VIPER-UPS) to allow VIPER system to continue to operate without main power.
  - 24V power supply module with power cords for US, UK, and European power sockets.
  - Optional - high performance IBM J9 VM.
  - Quickstart tutorial guide.

- **Wind River VxWorks 5.5 development kit**
  Features of this kit are:
  - 400MHz PXA255 processor with 64MB DRAM & 32MB Flash memory.
  - VxWorks BSP for Tornado 2.2.1/VxWorks 5.5.1/Wind ML 3.0.2.
  - Pre-configured build of VxWorks, tailored specifically for the VIPER, pre-loaded into the 32MB Flash.
  - Rugged enclosure with optional NEC Q-VGA TFT color display and analog touchscreen.
  - Uninterruptible power supply (VIPER-UPS) to allow VIPER system to continue to operate without main power.
  - 24V power supply module with power cords for US, UK, and European power sockets.

Entry level development kits for VIPER or VIPER-Lite

The following entry level development kits are available:

- **Windows CE / CE 5.0 development kit**
  Features of this kit for VIPER or VIPER-Lite are:
  - 400MHz (VIPER) or 200MHz (VIPER-Lite) PXA255 processor with 64MB DRAM & 32MB Flash memory.
  - Pre-configured build of Windows CE 5.0 tailored specifically for the VIPER, pre-loaded into the 32MB Flash.
  - +5V PSU.
  - All cables for immediate operation and download.
  - Development kit documentation.
  - Optional VIPER-I/O module.

- **Embedded Linux development kit**
  Features of this kit for VIPER or VIPER-Lite are:
  - 400MHz (VIPER) or 200MHz (VIPER-Lite) PXA255 processor with 64MB DRAM & 32MB Flash memory.
  - Pre-configured build of Arcom's Embedded Linux, tailored specifically for the VIPER, pre-loaded into the 32MB Flash.
  - +5V PSU.
  - All cables for immediate operation and download.
  - Development kit documentation.
  - Optional VIPER-I/O module.

Product handling and environmental compliance

Anti-static handling

This board contains CMOS devices that could be damaged in the event of static electricity discharged through them. At all times, please observe anti-static precautions when handling the board. This includes storing the board in appropriate anti-static packaging and wearing a wrist strap when handling the board.

Packaging

Please ensure that should a board need to be returned to Arcom, it is adequately packed, preferably in the original packing material.

Electromagnetic compatibility (EMC)

The VIPER is classified as a component with regard to the European Community EMC regulations and it is the users responsibility to ensure that systems using the board are compliant with the appropriate EMC standards.

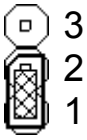
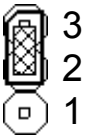
RoHS Compliance

The European RoHS Directive (Restriction on the use of certain Hazardous Substances – Directive 2002/95/EC) limits the amount of 6 specific substances within the composition of the product. The VIPER, VIPER-Lite, and associated accessory products are available as RoHS-6 compliant options and are identified by a -R6 suffix in the product order code. A full RoHS Compliance Materials Declaration Form is included in Appendix F – RoHS-6 Compliance - Materials Declaration Form, page 108. Further information about RoHS compliance is available on the Arcom web site – http://www.arcom.com/RoHS_and_WEEE/.

Conventions

Symbols

The following symbols are used in this guide:

Symbol	Explanation
	Note - information that requires your attention.
	Tip - a handy hint that may provide a useful alternative or save time.
	Caution - proceeding with a course of action may damage your equipment or result in loss of data.
	Indicates that a feature is not available on the standard VIPER-Lite configuration. Arcom can provide custom configurations (subject to a minimum order quantity) for the VIPER-Lite populated with this feature. Please contact our Sales team (see Appendix A – Contacting Arcom, page 101) to discuss your requirements.
	Jumper is fitted.
	Jumper is not fitted.
	Jumper fitted on pins 1-2.
	Jumper fitted on pins 2-3.

Tables

With tables such as that shown below, the white cells show information relevant to the subject being discussed. Grey cells are not relevant in the current context.

Byte lane	Most Significant Byte								Least Significant Byte							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	-	-	-	-	-	-	-	-	-	-	-	-	-	RETRIG	AUTO_CLR	R_DIS
Reset	X	X	X	X	X	X	X	X	0	0	0	0	0	0	0	0

Relevant information

Getting started

Depending on the development kit purchased, a Quickstart Manual is provided for Windows CE, embedded Linux, or VxWorks to enable users to set-up and start using the board. Please read the relevant manual and follow the steps defining the set-up of the board. Once you have completed this task you will have a working VIPER system and can start adding further peripherals enabling development to begin.

This section provides a guide to setting up and using of some of the features of the VIPER. For more detailed information on any aspect of the board see Detailed hardware description, page 18.

Using the VIPER

Using the CompactFLASH™ socket

The VIPER is fitted with a Type I/II CompactFLASH socket mounted on the topside of the board. The socket is connected to Slot 0 of the PXA255 PC card interface. It supports 3.3V Type I and II CompactFLASH cards for both memory and IO. The VIPER supports hot swap changeover of the cards and notification of card insertion.

RedBoot supports ATA type CompactFlash cards. Files can be read providing the card is formatted with an EXT2 file system. Eboot cannot boot from CompactFlash.

5V CompactFLASH is not supported.

The CompactFLASH card can only be inserted one way into the socket. The correct orientation is for the top of the card, i.e. with the normal printed side face down to the PCB.

Using the serial interfaces (RS232/422/485)

The five serial port interfaces on the VIPER are fully 16550 compatible. Connection to the serial ports is made via a 40-way boxed header. The pin assignment of this header has been arranged to enable 9-way IDC D-Sub plugs to be connected directly to the cable. See the section PL4 – COMS ports, page 89, for pin assignment and connector details.

A suitable cable for COM1 is provided as part of the development kit. The D-Sub connector on this cable is compatible with the standard 9-way connector on a desktop computer.

COM4 (RS232) and COM5 (RS422/485) are not available on the standard VIPER-Lite configuration. Arcom can provide custom configurations (subject to a minimum order quantity) for the VIPER-Lite populated with this feature. Please contact our Sales team (see Appendix A – Contacting Arcom, page 101) to discuss your requirements.

Using the audio features

There are four audio interfaces supported on the VIPER: amp out, line out, line in, and microphone. The line in, line out, and amp interfaces support stereo signals and the microphone provides a mono input. The amplified output is suitable for driving an 8Ω load with a maximum power output of 250mW per channel. Connections are routed to PL6 - see the sections Audio (page 56) and PL6 – Audio connector (page 91) for further details.

Using the USB host

The standard USB connector is a 4-way socket, which provides power and data signals to the USB peripheral. The 10-way header PL7 has been designed to be compatible with PC expansion brackets that support two USB sockets. See the sections USB host interface (page 60) and PL7 – USB connector (page 91) for further details.

Using the USB client

The VIPER board can be used as USB client and connected to a PC via a USB cable. The USB cable should be plugged into PL17 header. See the sections USB client interface (page 61) and PL17 – USB client connector (page 95) for further details.

Using the Ethernet interface

The SMSC LAN91C111 10/100BaseTX Ethernet controller is configured by the RedBoot bootloader for embedded Linux or VxWorks, and by Eboot for Windows CE.

Connection is made via connector PL1. A second connector PL2 provides activity and link status outputs for control LEDs. See the sections 10/100BaseTX Ethernet (page 62), PL1 – 10/100BaseTX Ethernet connector (page 87) and PL2 – Ethernet status LEDs connector (page 87) for further details.

The Ethernet port may be connected to an ETHER-BREAKOUT module to provide a standard RJ45 port connector, see section Ethernet breakout board, page 62 for further details.

Using the PC/104 expansion bus

PC/104 modules can be used with the VIPER to add extra functionality to the system. This interface supports 8/16 bit ISA bus style peripherals.

Arcom has a wide range of PC/104 modules, which are compatible with the VIPER. These include modules for digital I/O, analog I/O, motion control, CAN bus, serial interfaces, etc. Please contact the Arcom sales team if a particular interface you require does not appear to be available as these modules are in continuous development. Contact details are provided in Appendix A – Contacting Arcom, page 101.

In order to use a PC/104 board with the VIPER it should be plugged into PL11 for 8-bit cards and PL11/PL12 for 8/16-bit cards. See the sections PC/104 interface (page 67) and PL11 & PL12 – PC/104 connectors (page 94) for further details.

The ISA interface on the VIPER does not support DMA or shared interrupts. See the section Interrupt assignments, page 30, for details about PC/104 interrupt use.

The VIPER provides +5V to a PC/104 add-on board via the PL11 and PL12 connectors. If a PC/104 add-on board requires a +12V supply, then +12V must be supplied to the VIPER power connector PL16 pin 4. If –12V or –5V are required, these must be supplied directly to the PC/104 add-on board.

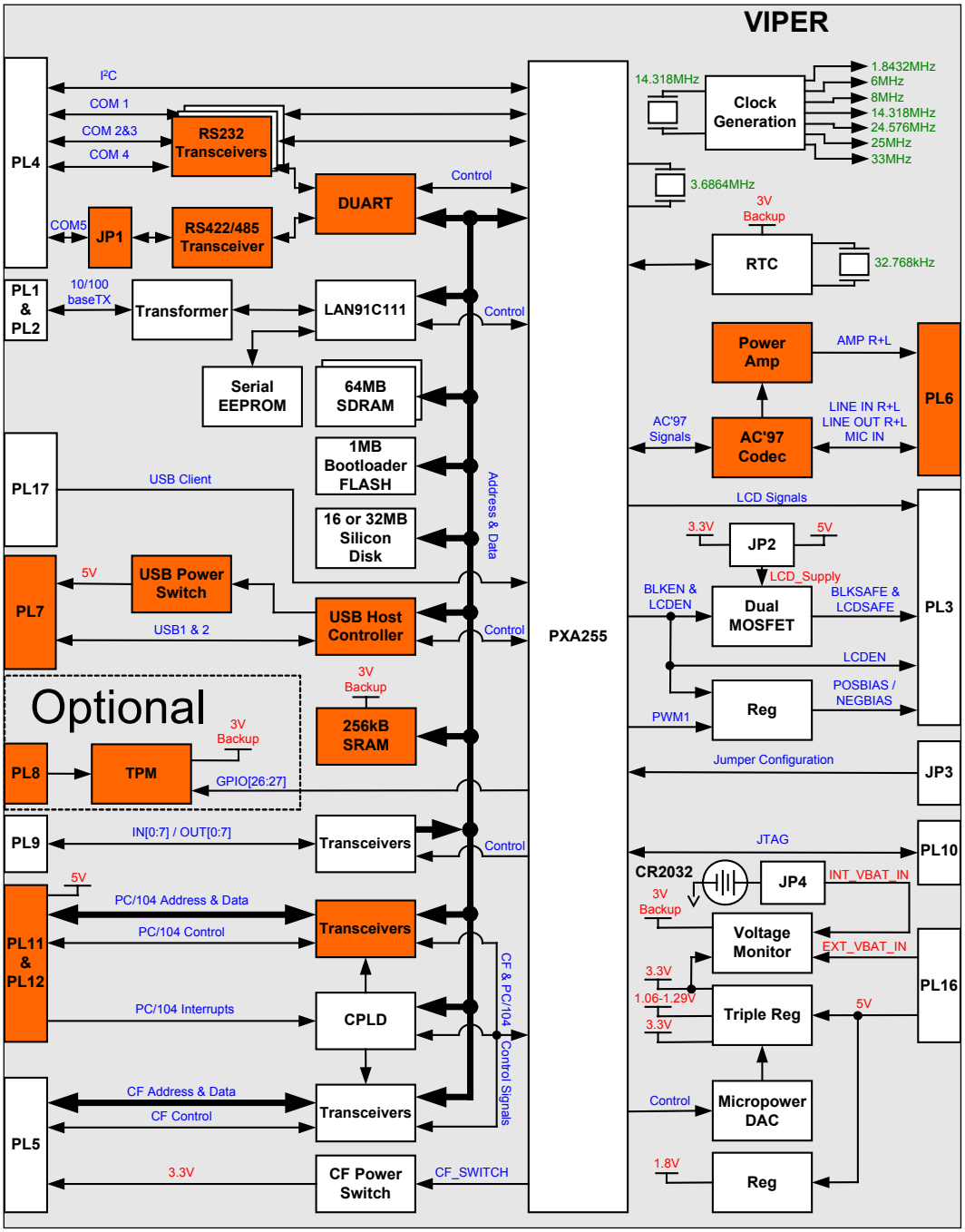
The VIPER is available with non-stack through connectors by special order. Contact Arcom (see Appendix A – Contacting Arcom, page 101, for more details.

Detailed hardware description

The following section provides a detailed description of the functions provided by the VIPER. This information may be required during development after you have started adding extra peripherals or are starting to use some of the embedded features.

VIPER block diagram

The diagram below illustrates the functional organization of the VIPER PC/104 SBC. Functions that are not available with the standard VIPER-Lite are highlighted in orange.



VIPER address map

	PXA255 chip select	Physical address	Bus/register width	Description
	-	0xA4000000 – 0xFFFFFFFF	-	Reserved
	SDCS0	0xA0000000 – 0xA3FFFFFC	32-bit	SDRAM, IC2&3
	-	0x4C000000 – 0x9FFFFFFF	-	Reserved
	NA	0x48000000 – 0x4BFFFFFF	32-bit	Memory Control Registers[1]
	NA	0x44000000 – 0x47FFFFFF	32-bit	LCD Control Registers[1]
	NA	0x40000000 – 0x43FFFFFF	32-bit	PXA255 Peripherals[1]
	-	0x3C200400 – 0x3FFFFFFF	-	Reserved
VL	NA	0x3C000000 – 0x3C1FFFFF	8/16-bit	PC/104 Memory Space
	-	0x30000400 – 0x3BFFFFFF	-	Reserved
VL	NA	0x30000000 – 0x300003FF	8/16-bit	PC/104 I/O Space
	NA	0x20000000 – 0x2FFFFFFF	32-bit	CompactFLASH, PL5
	-	0x14880000 – 0x1FFFFFFF	-	Reserved
VL	CS5	0x14800000 – 0x1487FFFF	16-bit	SRAM (see page 28)
	-	0x14500002 – 0x47FFFFFF	-	Reserved
	CS5	0x14500000 – 0x14500001	16-bit	General purpose I/O (see page 57)
	-	0x14300020 – 0x144FFFFF	-	Reserved
VL	CS5	0x14300010 – 0x1430001F	16-bit	COM4 (see page 65)
VL	CS5	0x14300000 – 0x1430000F	16-bit	COM5 (see page 65)
	-	0x14100006 – 0x142FFFFF	-	Reserved
VL	CS5	0x14100004 – 0x14100005	16-bit	PC104I2 Register (see page 31)
VL	CS5	0x14100002 – 0x14100003	16-bit	ICR Register (see page 31)
VL	CS5	0x14100000 – 0x14100001	16-bit	PC104I1 Register (see page 31)
	-	0x10000004 – 0x140FFFFF	-	Reserved
	CS4	0x10000000 – 0x100007FF	32-bit	Ethernet Data port
	-	0x0C000004 – 0x0FFFFFFF	-	Reserved
VL	CS3	0x0C000000 – 0x0C000002	16-bit	USB Host Controller
	-	0x08000310 – 0x0BFFFFFF	-	Reserved
	CS2	0x08000300 – 0x0800030E	16-bit	Ethernet I/O Space
	-	0x06000000 – 0x080002FF	-	Reserved
	CS1	0x04000000 – 0x05FFFFFE	16-bit	FLASH Memory / Silicon Disk
	-	0x00100000 – 0x03FFFFFF	-	Reserved
	CS0	0x00000000 – 0x000FFFFE	16-bit	Bootloader FLASH

[1] Details of the internal registers are in the Intel Developer Manual on the Development Kit CD.

Translations made by the MMU

For details of translations made by the MMU by Redboot for embedded Linux, please refer to the VIPER Embedded Linux AEL Technical Manual.

For details of translations made by the MMU by Redboot for VxWorks, please refer to the VIPER VxWorks Quickstart and Technical Manual.

For details of translations made by the MMU for Windows CE, please check the Windows CE documentation for more information about memory mapping. One source of this information is on the MSDN web site (www.msdn.microsoft.com) under *Windows CE Memory Architecture*.

PXA255 processor

The PXA255 is a low power ARM (version 5TE) instruction set compliant RISC processor. The PXA255 does not include a floating-point unit. The device does, however, contain a DSP co-processor to enhance multimedia applications.

The VIPER is fitted with a 400MHz PXA255 variant and the VIPER-Lite is fitted with a 200MHz PXA255 variant. The clock source for these is a 3.6864 MHz clock, which generates all the high-speed clocks within the device. The default run mode frequency is 400MHz for the VIPER and 200MHz for the VIPER-Lite. Currently embedded Linux and VxWorks supports changing the operating frequency and Windows CE will provide support shortly. Please refer to the relevant operating system technical manual to select an alternative operating frequency.

The processor has two supply inputs: I/O and core generated on the VIPER from the main +5V supply input. The I/O supply is powered from +3.3V, and the core is powered from a +1.06 to +1.3V adjustable supply. See the section Processor power management, page 81, for operation details.

The PXA255 has an integrated memory and CompactFlash controller with 100 MHz memory bus, 32KB data and 32KB instruction caches, and 2KB mini data cache for streaming data.

The PXA255 provides up to 85 GPIO pins, many of which have been configured for alternative functions like the AC'97 and PC card/CompactFLASH interfaces. Details of these pin configurations are provided in the section PXA255 GPIO pin assignments, page 22.

The PXA255 also has the following features that can be used on the VIPER:

- Peripheral Control Module:
  - 16 channel configurable DMA controller (for internal use only).
  - Integrated LCD controller with unique DMA for fast color screen support.
  - Serial ports including AC'97, 3 UARTs, and enhanced USB end point interface.

- System Control Module:
  - General-purpose interruptible I/O ports.
  - Real time clock.
  - Watchdog.
  - Interval timers.
  - Power management controller.
  - Interrupt controller.
  - Reset controller.
  - Two on-chip oscillators.

The PXA255 processor is packaged in a 256-pin PBGA, which is attached to the board during the assembly process.

The PXA255 processor is a low power device and does not require a heat sink for temperatures up to 70°C (85°C for the industrial variant).

PXA255 GPIO pin assignments

The following table summarizes the use of the 85 PXA255 GPIO pins, their direction, alternate function, and active level.

For embedded Linux the GPIO pins are setup by Redboot. Under VxWorks and Windows CE, they are setup by the OS and not by the bootloader.

Key:

AF Alternate function.
Dir Pin direction.
Active Function active level or edge.
Sleep Pin state during sleep mode (all Hi-Z states are to '1' during sleep).

GPIO No	AF	Signal name	Dir	Active	Sleep	Function	See section...
0	0	ETHER_INT	Input	↑	Input	Ethernet Interrupt	
1	0	PC/104_IRQ	Input	See page 30	Input	CPLD Interrupt	Interrupt assignments (page 30)
2	0	USB_IRQ	Input	↓	Input	USB Interrupt	
3	0	UART_INT1	Input	↑	Input	COM 5 Interrupt	
4	0	UART_INT2	Input	↑	Input	COM 4 Interrupt	
5	0	Reserved	Input	NA	Input	Reserved	Reserved – LK2 (page 98)
6	0	PSU_DATA	Output	NA	0	Microprocessor Core Voltage DAC Data	Processor power management (page 81)
7	0	USER_CONFIG1	Input	NA	Input	User Config 1, Jumper LK3	User configurable jumper 1 – LK3 (page 98)
8	0	CF_RDY	Input	NA	Input	CompactFLASH Ready/nBusy	Interrupt assignments, (page 30 and CompactFLASH page 28)
9	0	BLKEN	Output	High	0	LCD Backlight Enable	LCD backlight enable (page 37)
10	0	LCDEN	Output	High	0	LCD Logic Supply Enable	LCD logic supply enable (page 37)
11	0	PSU_CLK	Output	↑	0	Microprocessor Core Voltage DAC Clock	Processor power management (page 81)
12	0	SHDN	Output	High	1	COM 1, 2, 3 & 4 UART Shutdown	UART power management (page 83)
13	0	USB_WAKEUP	Output	High	0	Wake Up USB Host from suspend	USB power management (page 83)

continued…

GPIO No	AF	Signal name	Dir	Active	Sleep	Function	See section...
14	0	FLASH_ STATUS	Input	NA	Input	Bootloader FLASH Status, Ready / nBusy	Interrupt assignments (page 30) and FLASH memory/silicon disk (page 27)
15	2	CS1	Output	Low	Hi-Z	Chip Select 1	VIPER address map (page 19)
16	2	PWM0	Output	See inverter datasheet	0	Backlight Brightness On/Off or variable if PWM	LCD backlight brightness control (page 37)
17	2	PWM1	Output	NA	0	STN Bias	STN BIAS voltage (page 38)
18	1	ARDY	Input	Low	Input	10/100 Ethernet PHY Ready	-
19	0	PSU_nCS_LD	Output	Low	0	Microprocessor Core Voltage DAC Chip Select	Processor power management (page 81)
20	0	OUT0					
21	0	OUT1					
22	0	OUT2					
23	0	OUT3	Output	User Config	0	User Config	General purpose I/O (page 57)
24	0	OUT4					
25	0	OUT5					
26	0	OUT6					
27	0	OUT7					
VL 28	1	AC97_BITCLK	Input	↑	Input	BITCLK	
VL 29	1	AC97_IN	Input	NA	Input	SDATA_IN0	-
VL 30	2	AC97_OUT	Output	NA	0	SDATA_OUT	
VL 31	2	AC97_SYNC	Output	↑	0	SYNC	
32	0	CF_DETECT	Input	↓	Input	CF Detection	Interrupt assignments (page 30) and CompactFLASH (page 28)
33	2	CPLDCS	Output	Low	Hi-Z	Chip Select 5	VIPER address map, (page 19)

continued…

GPIO No	AF	Signal name	Dir	Active	Sleep	Function	See section...
34	1	RXD1	Input	NA	Input	COM1 Receive Data	
35	1	CTS1	Input	NA	Input	COM1 Clear To Send	
36	1	DCD1	Input	NA	Input	COM1 Data Carrier Detect	
37	1	DSR1	Input	NA	Input	COM1 Data Sender Ready	
38	1	RI1	Input	NA	Input	COM1 Ring Indicator	
39	2	TXD1	Output	NA	0	COM1 Transmit Data	
40	2	DTR1	Output	NA	0	COM1 Data Terminal Ready	Serial COMs ports (page 64) and PL4 – COMS ports (page 89).
41	2	RTS1	Output	NA	0	COM1 Request To Send	
42	1	RXD2	Input	NA	Input	COM2 Receive Data	
43	2	TXD2	Output	NA	0	COM2 Transmit Data	
44	1	CTS2	Input	NA	Input	COM2 Clear To Send	
45	2	RTS2	Output	NA	0	COM2 Request To Send	
46	2	RXD3	Input	NA	Input	COM3 Receive Data	
47	1	TXD3	Output	NA	0	COM3 Transmit Data	
48	2	CB_POE	Output	Low	1	Socket 0 & 1 Output Enable	
49	2	CB_PWE	Output	Low	1	Socket 0 & 1 Write Enable	
50	2	CB_PIOR	Output	Low	1	Socket 0 & 1 I/O Read	-
51	2	CB_PIOW	Output	Low	1	Socket 0 & 1 I/O Write	
52	2	CB_PCE1	Output	Low	1	Socket 0 & 1 Low Byte Enable	
53	2	CB_PCE2	Output	Low	1	Socket 0 & 1 High Byte Enable	
54	2	CB_PKTSEL	Output	NA	1	PSKTSEL 0 = Socket 0 Select / 1 = Socket 1 Select	-
55	2	CB_PREG	Output	Low	1	PREG	-
56	1	CB_PWAIT	Input	Low	Input	PWAIT	-
57	1	CB_PIOIS16	Input	Low	Input	IOIS16	

continued…

GPIO No	AF	Signal name	Dir	Active	Sleep	Function	See section...
58	2	LCD_D0	Output	NA	0	LCD Data Bit 0	
59	2	LCD_D1	Output	NA	0	LCD Data Bit 1	
60	2	LCD_D2	Output	NA	0	LCD Data Bit 2	
61	2	LCD_D3	Output	NA	0	LCD Data Bit 3	
62	2	LCD_D4	Output	NA	0	LCD Data Bit 4	
63	2	LCD_D5	Output	NA	0	LCD Data Bit 5	
64	2	LCD_D6	Output	NA	0	LCD Data Bit 6	
65	2	LCD_D7	Output	NA	0	LCD Data Bit 7	
66	2	LCD_D8	Output	NA	0	LCD Data Bit 8	
67	2	LCD_D9	Output	NA	0	LCD Data Bit 9	
68	2	LCD_D10	Output	NA	0	LCD Data Bit 10	Flat panel display support (page 34) and PL3 – LCD connector (page 88)
69	2	LCD_D11	Output	NA	0	LCD Data Bit 11	
70	2	LCD_D12	Output	NA	0	LCD Data Bit 12	
71	2	LCD_D13	Output	NA	0	LCD Data Bit 13	
72	2	LCD_D14	Output	NA	0	LCD Data Bit 14	
73	2	LCD_D15	Output	NA	0	LCD Data Bit 15	
74	2	LCD_FCLK	Output	NA	0	LCD Frame Clock (STN) Vertical Sync (TFT)	
75	2	LCD_LCLK	Output	NA	0	LCD Line Clock (STN) / Horizontal Sync (TFT)	
76	2	LCD_PCLK	Output	NA	0	LCD Pixel Clock (STN) / Clock (TFT)	
77	2	LCD_BIAS	Output	NA	0	LCD Bias (STN) / Date Enable (TFT)	
78	2	ETHERCS2	Output	Low	Hi-Z	Chip Select 2	VIPER address map (page 19)
79	2	USBCS	Output	Low	Hi-Z	Chip Select 3	
80	2	ETHERCS1	Output	Low	Hi-Z	Chip Select 4	
81	0	SDRAM	Input	NA	Input	SDRAM Size Detection 0 = 64MB, 1 = 16MB	-
82	0	CF_SWITCH	Output	High	0	CompactFLASH Power Switch Enable	CompactFLASH (page 28) and CompactFLASH power management (page 83)
83	0	RTC_IO	Bidirec-tional	NA	0	RTC Data	Real time clock (page 26)
84	0	RTC_CLK	Output	↓	0	RTC Clock	

Real time clock

There are two RTCs on the VIPER. Under embedded Linux and VxWorks the internal RTC of the PXA255 should only be used for power management events, and an external Dallas DS1338 RTC should be used to keep the time and date. Under Windows CE the time and date stamps are copied from the external RTC to the internal RTC of the PXA255, to run the RTC internally.

The accuracy of the DS1338 RTC is based on the operation of the 32.768KHz watch crystal. Its calibration tolerance is ±20ppm, which provides an accuracy of +/-1 minute per month if the board is in an ambient environment of +25°C. When the board is operated outside this temperature then the accuracy may be degraded by -0.035ppm/ °C² ±10% typical. The watch crystal's accuracy will age by ±3ppm max in the first year, then ±1ppm max in the year after, and logarithmically decreasing in subsequent years.

The following PXA255 GPIO pins are used to emulate the I²C interface to the DS1338 RTC:

PXA255 Pin	Function
GPIO84	Clock (100kHz max)
GPIO83	Data

The DS1338 RTC also contains 56 bytes of RAM, which can be used for any user data that needs to be recoverable on power-up.

To ensure the DS1338 RTC doesn't lose track of the date and time when the 5V supply is powered-down, the onboard battery must be fitted. See the section Battery backup, page 73, for details.

Watchdog timer

The PXA255 contains an internal watchdog timer, which can be used to protect against erroneous software. Timeout periods can be adjusted from 271ns to 19 minutes 25 seconds. When a timeout occurs the board is reset. On reset the watchdog timer is disabled until enabled again by software.

For further details see the Arcom Operating System Technical Manual and the PXA255 Developer's Manual on the Development Kit CD.

Memory

The VIPER has four types of memory fitted:

- 1MB of bootloader FLASH containing Redboot to boot embedded Linux or VxWorks, or Eboot to boot Windows CE.
- A resident FLASH disk containing the OS and application images.
- SDRAM for system memory.
- VL 256KB Static RAM (SRAM).

A 1MB Bottom Boot FLASH EPROM device, arranged as 512Kbit x 16, is used as the bootloader FLASH. It holds Redboot (for embedded Linux or VxWorks) or Eboot (for Windows CE), together with configuration information. When the microprocessor comes out of reset it boots the relevant bootloader from here, which in turn boots up the OS from the FLASH memory/silicon disk. Whenever the Bootloader FLASH memory is accessed the FLASH access LED illuminates.

FLASH memory/silicon disk

The VIPER supports 16MB or 32MB of Intel StrataFLASH memory for the OS and application images. The FLASH memory is arranged as 64Mbit x 16-bits (16MB device) or as 128Mbit x 16-bits (32MB device) respectively.

The FLASH memory array is divided into equally sized symmetrical blocks that are 64-Kword in size. A 128Mbit device contains 128 blocks, and 256Mbit device contains 256 blocks. Flash cells within a block are organized by rows and columns. A block contains 512 rows by 128 words. The words on a row are divided into 16 eight-word groups.

The PXA255 GPIO14 pin is connected to the FLASH memory status output. This pin can be used to generate an interrupt to indicate the completion of a CFI command.

Whenever the FLASH memory is accessed the FLASH access LED illuminates.

SDRAM interface

There are two memory configurations supported by the VIPER: 16MB or 64MB of SDRAM located in Bank 0. The SDRAM is configured as 4MB x 32-bits (16MB) or 16MB x 32-bits (64MB), by 2 devices with 4 internal banks of 1MB or 4MB x 16-bits.

These are surface mount devices soldered to the board and cannot be upgraded. RedBoot (embedded Linux and VxWorks) automatically detects the amount of memory fitted to the board, and configures the SDRAM controller accordingly. For Windows CE applications the SDRAM memory will always be 64MB.

The SDRAM controller supports running the memory at frequencies between 50MHz and 99.5MHz (default). This can be configured to achieve the optimum balance between power consumption and performance.

Static RAM

The VIPER has a 256KB SRAM device fitted, arranged as 256Kbit x 8-bits. Access to the device is on 16-bit boundaries; whereby the least significant byte is the SRAM data and the 8-bits of the most significant byte are don't care bits. The reason for this is that the PXA255 is not designed to interface to 8-bit peripherals. This arrangement is summarized in the following data bus table:

Most Significant Byte								Least Significant Byte							
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Don't Care								SRAM Data							

The SRAM is non-volatile while the onboard battery is fitted.

CompactFLASH

The CompactFLASH connector PL5 is interfaced to Slot 0 of the PXA255 PC card controller, and appears in PC card memory space socket 0.

This is a hot swappable 3.3V interface, controlled by the detection of a falling edge on GPIO32 when a CompactFLASH card has been inserted. On detection set GPIO82 to logic '1' to enable the 3.3V supply to the CompactFLASH connector. The CompactFLASH (RDY/nBSY) signal interrupts on GPIO8.

Address	Region name
0x2C000000 – 0x2FFFFFFF	Socket 0 Common Memory Space
0x28000000 – 0x2BFFFFFF	Socket 0 Attribute Memory Space
0x24000000 – 0x27FFFFFF	Reserved
0x20000000 – 0x23FFFFFF	Socket 0 I/O Space

Many CF+ cards require a reset once they have been inserted. The CF reset must remain high (inactive) for 1ms after power has been applied to the CF socket, and then go low (active) for at least 10µs.

To reset the CompactFlash socket independently set the CF_RST bit to '1' in the ICR register located at offset 0x100002 from CS5 (0x14000000). To clear the CompactFlash reset write a '0' to the CF_RST bit.

Interrupt configuration and reset register [ICR]

Byte lane	Most Significant Byte								Least Significant Byte							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	-	-	-	-	-	-	-	-	-	-	-	-	$CF\_\overline{RST}$	R_DIS	AUTO_CLR	RETRIG
Reset	X	X	X	X	X	X	X	X	0	0	0	0	0	0	0	0
R/W	-	-	-	-	-	-	-	-	R				R/W			
Address	0x14100002															

ICR Bit Functions

Bit	Name	Value	Function
0	RETRIG	0	No interrupt retrigger (embedded Linux and VxWorks).
		1	Interrupt retrigger (Windows CE).
1	AUTO_CLR	0	No auto clear interrupt / Toggle GPIO1 on new interrupt.
		1	Auto clear interrupt / Low to high transition on GPIO1 on First Interrupt.
2	R_DIS	0	Board reset normal
		1	Board reset disable
3	CF_RST	0	CompactFlash reset by board reset
		1	Reset CompactFlash
4 - 7	-	X	No function.

Interrupt assignments

Internal interrupts

For details on the PXA255 interrupt controller and internal peripheral interrupts please see the PXA255 Developer's Manual on the Development Kit CD.

External interrupts

The following table lists the PXA255 signal pins used for generating external interrupts.

PXA255 Pin	Peripheral	Active
GPIO0	Ethernet	↑
GPIO1	PC/104 interrupt controller	See PC/104 interrupts, page 30
GPIO2	USB	↓
GPIO3	COM5	↑
GPIO4	COM4	↑
GPIO8	CompactFLASH RDY/nBSY	Ready = ↑ , Busy = ↓
GPIO14	FLASH (OS)	Ready = ↑ , Busy = ↓
GPIO32	CompactFLASH card detect	↓

PC/104 interrupts

The PC/104 interrupts are logically OR'ed together so that any interrupt generated on the PC/104 interface generates an interrupt input on GPIO1.

The PC/104 interrupting source can be identified by reading the PC104I1 & 2 registers (PC104I2 is not available under Windows CE as all interrupt sources are fully utilized) located at offset 0x100000 and 0x100004 respectively from CS5 (0x14000000). The registers indicate the status of the interrupt lines at the time the register is read. The relevant interrupt has its corresponding bit set to '1'. The PXA255 is not designed to interface to 8-bit peripherals, so only the least significant byte from the word contains the data.

PC/104 interrupt register [PC104I1]

Byte lane	Most Significant Byte								Least Significant Byte							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	-	-	-	-	-	-	-	-	IRQ12	IRQ11	IRQ10	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3
Reset	X	X	X	X	X	X	X	X	0	0	0	0	0	0	0	0
R/W	-	-	-	-	-	-	-	-	R/W							
Address	0x14100000															

PC/104 interrupt register [PC104I2] (not available under Windows CE)

Byte lane	Most Significant Byte								Least Significant Byte							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	-	-	-	-	-	-	-	-	-	-	-	-	-	IRQ15	IRQ14	IRQ9
Reset	X	X	X	X	X	X	X	X	0	0	0	0	0	0	0	0
R/W	-	-	-	-	-	-	-	-	R					R/W		
Address	0x14100004															

The ICR Register located at offset 0x100002 from CS5 (0x14000000) must be set-up correctly for the OS running. The PC/104 interrupts are signaled and handled slightly differently between embedded Linux / VxWorks and Windows CE. See the following relevant subsections for specific PC/104 details for the target OS.

Interrupt configuration and reset register [ICR]

Byte lane	Most Significant Byte								Least Significant Byte							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	-	-	-	-	-	-	-	-	-	-	-	-	$\overline{\text{CF\_RST}}$	R_DIS	AUTO_CLR	RETRIG
Reset	X	X	X	X	X	X	X	X	0	0	0	0	0	0	0	0
R/W	-	-	-	-	-	-	-	-	R				R/W			
Address	0x14100002															

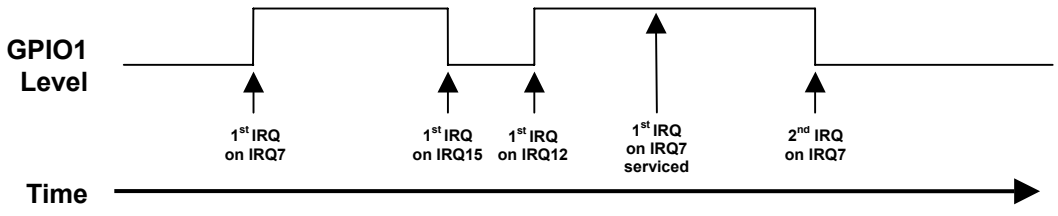
ICR Bit Functions

Bit	Name	Value	Function
0	RETRIG	0	No interrupt retrigger (embedded Linux and VxWorks)
		1	Interrupt retrigger (Windows CE)
1	AUTO_CLR	0	No auto clear interrupt / Toggle GPIO1 on new interrupt (embedded Linux and VxWorks)
		1	Auto clear interrupt / pulse low for 1.12µs on GPIO1 on new interrupt from a new interrupt source (Windows CE)
2	R_DIS	0	Board reset normal
		1	Board reset disable (Set before entering CPU sleep)
3	CF_RST	0	CompactFlash reset controlled by board reset
		1	Reset CompactFlash
4 - 7	-	X	No function

PC/104 interrupts under embedded Linux and VxWorks

Leave the ICR register set to its default value, so that a new interrupt causes the microprocessor PC/104 interrupt pin GPIO1 to be toggled for every new interrupt on a different PC/104 interrupt source. Ensure the GPIO1 input is set up in a level triggered mode. The retrigger interrupt function is not required for embedded Linux or VxWorks.

The following diagram gives an example of how the PC/104 interrupt on GPIO1 behaves over time when the ICR AUTO_CLR bit is set to '0':



Once the VIPER microprocessor has serviced a PC/104 interrupt, clear the corresponding bit in the corresponding PC104I register by writing '1' to it.

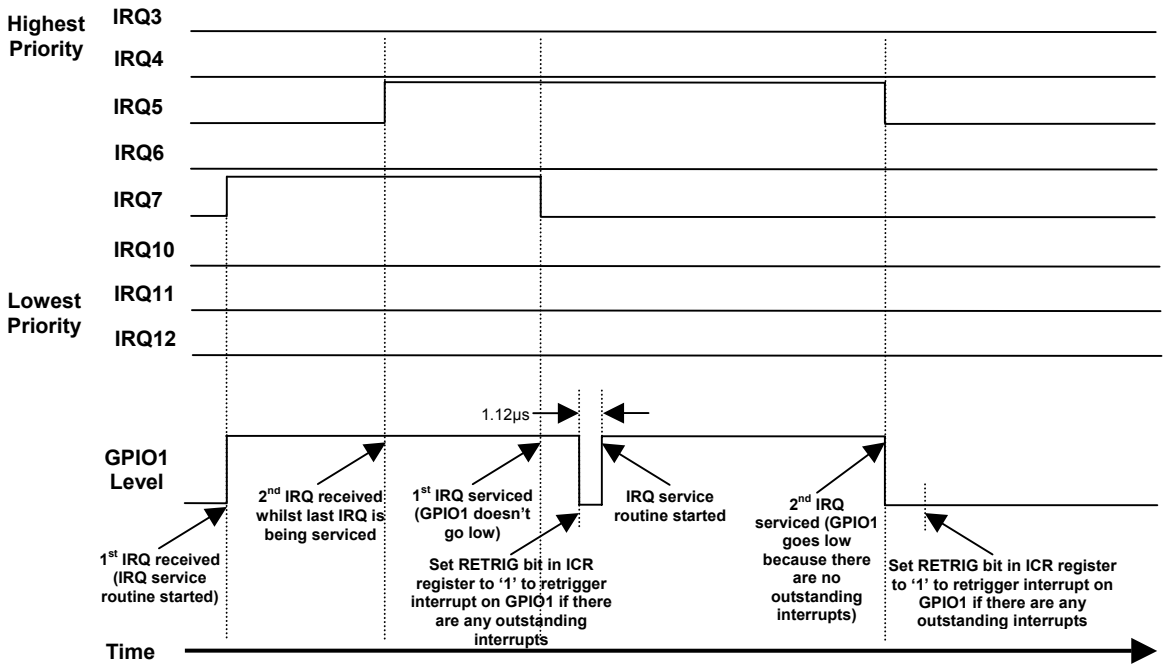
PC/104 interrupts under Windows CE

Write 0x2 to the ICR Register so that the first PC/104 interrupt source causes the PXA255 PC/104 interrupt pin GPIO1 to receive a low to high transition. When the first PC/104 interrupt occurs the Interrupt service routine will start polling through the PC/104 interrupt sources in the PC104I1 register. The first bit it sees set to a '1', sets a semaphore to make a program run to service the corresponding interrupt.

Once this program has serviced the interrupt the interrupting source returns its interrupt output to the inactive state ('0') if it hasn't requested another interrupt whilst the microprocessor serviced the last interrupt. Once this happens the corresponding bit in the PC104I1 register shall be automatically cleared. Each PC/104 board requesting an interrupt shall keep its interrupt in the active state ('1') until the interrupt has been serviced by the microprocessor. When there are no interrupts outstanding the level of the PC/104 interrupt on GPIO1 shall automatically return to logic '0'. If it is still '1' then there are interrupts outstanding, which would have occurred during the servicing of the last interrupt.

To capture any interrupts that could have occurred whilst the last interrupt was serviced, the retrigger interrupt bit in the ICR register is set to '1' to retrigger a low to high transition on GPIO1 to restart the interrupt polling mechanism if there are any outstanding interrupts.

The diagram below explains how the PC/104 interrupt on GPIO1 behaves over time when the ICR AUTO_CLR bit is set to '1':



PC/104 IRQ9, IRQ14, and IRQ15 are not available under Windows CE as all interrupt sources are fully utilized; therefore the PC104I2 register is disabled for Windows CE.

Flat panel display support

The PXA255 processor contains an integrated LCD display controller that permits 1, 2, and 4-bit gray-scale, and 8 or 16-bit color pixels. A 256-byte palette RAM provides flexible color mapping capabilities. The LCD display controller supports active (TFT) and passive (STN) LCD displays.

The PXA255 can drive displays with a resolution up to 800x600, but as the PXA255 has a unified memory structure, the bandwidth to the application decreases significantly. If the application makes significant use of memory, such as when video is on screen, you may also experience FIFO under-run to the LCD causing the frames rates to drop or display image disruption. Reducing the frame rate to the slowest speed possible gives the maximum bandwidth to the application. The display quality for an 800x600 resolution LCD is dependant on the compromises that can be made between the LCD refresh rate and the application. The PXA255 is best suited to 320x240 and 640x480 resolution displays.

A full explanation of the graphics controller operation can be found in the PXA255 data sheets included on the support CD.

The flat panel data and control signals are routed to PL3. See the section PL3 – LCD connector, page 88, for pin assignment and part number details.

The VIPER-FPIF1 allows the user to easily wire-up a new panel using pin and crimp style connectors. Contact Arcom (see Appendix A – Contacting Arcom, page 101) for purchasing information.

A list of proven Flat Panel displays is included on the VIPER product page. Click on the *Flat Panel Display Options* tab for up-to-date details.

The following tables provide a cross-reference between the flat panel data signals and their function when configured for different displays.

TFT panel data bit mapping to the VIPER

Panel data bus bit	18-bit TFT	12-bit TFT	9-bit TFT
FPD 15	R5	R3	R2
FPD 14	R4	R2	R1
FPD 13	R3	R1	R0
FPD 12	R2	R0	-
FPD 11	R1	-	-
GND	R0	-	-
FPD 10	G5	G3	G2
FPD 9	G4	G2	G1
FPD 8	G3	G1	G0
FPD 7	G2	G0	-
FPD 6	G1	-	-
FPD 5	G0	-	-
FPD 4	B5	B3	B2
FPD 3	B4	B2	B1
FPD 2	B3	B1	B0
FPD 1	B2	B0	-
FPD 0	B1	-	-
GND	B0	-	-

The PXA255 cannot directly interface to 18-bit displays, as its color palette RAM has 5 bits for red, 6 bits for green, and 5 bits for blue, since the human eye can distinguish more shades of green than of red or blue.

STN panel data bit mapping to the VIPER

Panel data bus bit	Dual scan color STN	Single scan color STN	Dual scan mono STN
FPD 15	DL7(G)	-	-
FPD 14	DL6(R)	-	-
FPD 13	DL5(B)	-	-
FPD 12	DL4(G)	-	-
FPD 11	DL3(R)	-	-
FPD 10	DL2(B)	-	-
FPD 9	DL1(G)	-	-
FPD 8	DL0(R)	-	-
FPD 7	DU7(G)	D7(G)	DL3
FPD 6	DU6(R)	D6(R)	DL2
FPD 5	DU5(B)	D5(B)	DL1
FPD 4	DU4(G)	D4(G)	DL0
FPD 3	DU3(R)	D3(R)	DU3
FPD 2	DU2(B)	D2(B)	DU2
FPD 1	DU1(G)	D1(G)	DU1
FPD 0	DU0(R)	D0(R)	DU0

Below is a table covering the clock signals required for passive and active type displays:

VIPER	Active display signal (TFT)	Passive display signal (STN)
PCLK	Clock	Pixel Clock
LCLK	Horizontal Sync	Line Clock
FCLK	Vertical Sync	Frame Clock
BIAS	DE (Data Enable)	Bias

The display signals are +3.3V compatible; the VIPER contains power control circuitry for the flat panel logic supply and backlight supply. The flat panel logic is supplied with a switched 3.3V (default) or 5V supply, see section LCD Supply Voltage – LK8 on JP2, page 100 for details. The backlight is supplied with a switched 5V supply for the inverter.

There is no on-board protection for these switched supplies! Care must be taken during power up/down to ensure the panel is not damaged due to the input signals being incorrectly configured.

Typically the power up sequence is as follows (please check the datasheet for the particular panel in use):

1 Enable display VCC.

2 Enable flat panel interface.

3 Enable backlight.

Power down is in reverse order.

LCD backlight enable

The PXA255 GPIO9 pin controls the LCD inverter supply voltage for the backlight. When GPIO9 is set to logic '1', the backlight supply BLKSAFE is supplied with 5V (turned on). The BLKEN signal on PL3 is the un-buffered GPIO9 signal. See the section PL3 – LCD connector, page 88, for PL3 pin assignment, connector, and mating connector details.

If you want to use a 12V backlight inverter, then the switched 5V supply on BLKSAFE or the control signal BLKEN can be used to control an external 12V supply to the inverter.

LCD logic supply enable

The PXA255 GPIO10 pin controls the supply voltage for the LCD logic. When GPIO10 is set to logic '1', the LCD supply LCDSAFE is supplied with 3.3V (turned on). See the section PL3 – LCD connector, page 88, for PL3 pin assignment, connector, and mating connector details.

The LCD supply may be changed to 5V by moving the jumper position of JP2 (see section LCD Supply Voltage – LK8 on JP2, page 100 for details). If the flat panel logic is powered from 5V, it must be compatible with 3.3V signaling. Please check the LCD panel datasheet for details.

LCD backlight brightness control

The control of the backlight brightness is dependant upon the type of backlight inverter used in the display. Some inverters have a 'DIM' function, which uses a logic level to choose between two levels of intensity. If this is the case then GPIO16 (Alternative Function 0) is used to set this. Other inverters have an input suitable for a pulse-width modulated signal; in this case GPIO16 should be configured as PWM0 (Alternative Function 2).

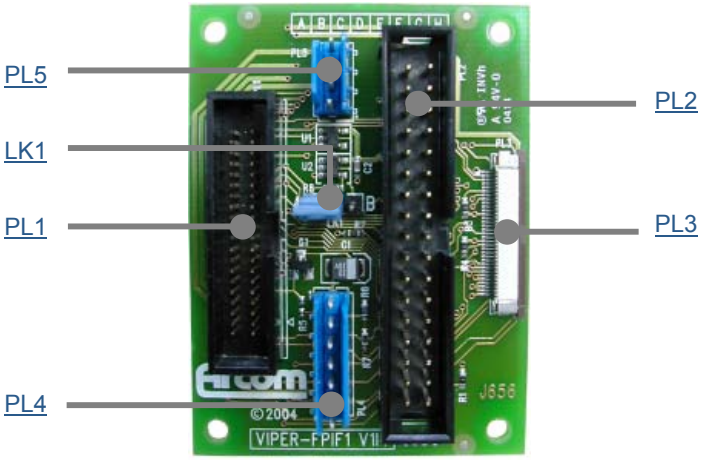
STN BIAS voltage

The VIPER provides a negative and a positive bias voltage for STN type displays. The negative and positive bias voltages are set to –22V and +22V respectively. Pin connections for these can be found in the section PL3 – LCD connector, page 88. Please contact Arcom for details of other bias voltages. Contact details are provided in Appendix A – Contacting Arcom, page 101.

Do not exceed 20mA load current.

VIPER-FPIF1 details

The VIPER-FPIF1 allows easy connection between the VIPER and a variety of TFT or STN LCD flat panel displays.



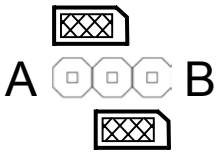
The connectors on the following pages are shown in the same orientation as the picture above.

Connector	Function
LK1	TFT clock delay selection
PL1	VIPER LCD cable connector
PL2	Generic LCD connector
PL3	Direct connection to a NEC NL3224BC35-20 5.5inch 320x240 TFT display
PL4	Connects to backlight inverter
PL5	STN bias voltages

VIPER-FPIF1 connectors

LK1 – TFT clock delay selection

It has been found that some TFT displays require a delay on the clock. If this is required fit the jumper in position A; if not, then fit in position B.

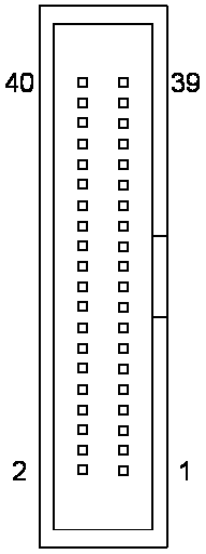


PL1 – VIPER LCD cable connector

Connector: Oupiin 3215-40GSB/SN, 40-way, 1.27mm (0.05”) x 2.54mm (0.1”) straight-boxed header

Mating connector: Oupiin 1203-40GB/SN (available from Arcom on request)

Pin	Signal name	Pin	Signal name
1	BLKEN#	2	BLKSAFE
3	GND	4	GND
5	NEGBIAS	6	LCDSAFE
7	GPIO16/PWM0	8	POSBIAS
9	GND	10	GND
11	FPD 0	12	FPD 1
13	FPD 2	14	FPD 3
15	GND	16	GND
17	FPD 4	18	FPD 5
19	FPD 6	20	FPD 7
21	GND	22	GND
23	FPD 8	24	FPD 9
25	FPD 10	26	FPD 11
27	GND	28	GND
29	FPD 12	30	FPD 13
31	FPD 14	32	FPD 15
33	GND	34	GND
35	FCLK / VSYNC	36	BIAS / DE
37	GND	38	GND
39	PCLK / CLOCK	40	LCLK / HSYNC



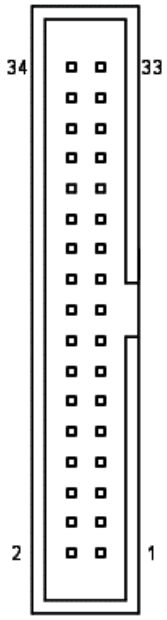
PL2 – Generic LCD connector

Connector: Taicom TI34BHS, 34-way, 2.54mm (0.1”) x 2.54mm (0.1”) straight-boxed header

Mating connector: Fujitsu FCN-723-B034/2

Mating connector crimps: Fujitsu FCN-723J-AU/Q. (As it is possible to connect a crimp type connector to PL2, a wide range of LCD displays can be connected with a custom cable)

Pin	Signal name	Pin	Signal name
1	GND	2	FPD 0
3	FPD 1	4	FPD 2
5	GND	6	FPD 3
7	FPD 4	8	FPD 5
9	FPD 6	10	GND
11	FPD 7	12	FPD 8
13	FPD 9	14	FPD 10
15	GND	16	GND
17	FPD 11	18	FPD 12
19	FPD 13	20	GND
21	FPD 14	22	FPD 15
23	GND	24	PCLK / CLOCK
25	GND	26	LCDSAFE
27	LCDSAFE	28	LCLK / HSYNC
29	FCLK / VSYNC	30	GND
31	BKLSAFE	32	BIAS / DE
33	NC	34	BKLEN#

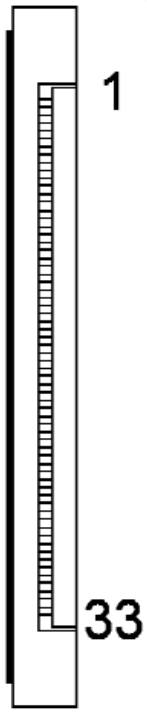


PL3 – Direct connection to a NEC NL3224BC35-20 5.5inch 320x240 TFT display

Connector: Oupiin 2345-33TD2/SN

Mating cable: Eunsung 0.5x33x190xAx0.035x0.3x5x5x10x10

Pin	Signal name	Pin	Signal name
1	GND	18	FPD 10
2	PCLK	19	GND
3	LCLK (HSYNC)	20	GND
4	FCLK (VSYNC)	21	FPD 0
5	GND	22	FPD 1
6	GND	23	FPD 2
7	FPD 11	24	FPD 3
8	FPD 12	25	FPD 4
9	FPD 13	26	GND
10	FPD 14	27	LBIAS
11	FPD 15	28	LCDSAFE
12	GND	29	LCDSAFE
13	FPD 5	30	GND
14	FPD 6	31	GND
15	FPD 7	32	GND
16	FPD 8	33	GND
17	FPD 9		



PL4 – Backlight inverter connector

Connector: FCI 76384-407LF

Mating connector: FCI 65240-007LF

Mating connector crimps: FCI 76357-401LF

Pin	Signal name
1	GND
2	PWM0
3	BKLEN#
4	GND
5	GND
6	BKLSAFE
7	BKLSAFE

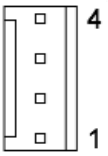
PL5 – STN Bias connector

Connector: FCI 76384-404LF

Mating connector: FCI 65240-004LF

Mating connector crimps: FCI 76357-401LF

Pin	Signal name
1	NEGBIAS
2	GND
3	GND
4	POSBIAS



FPIF-LVDS-TX details

The FPIF-LVDS-TX enables LVDS displays to be connected to the VIPER.

The FPIF-LVDS-TX in combination with the FPIF-LVDS-RX allows the VIPER to drive a TFT or STN LCD flat panel display up to 10 meters away.

When using the FPIF-LVDS-TX, ensure the VIPER JP2 jumper is set to select 3.3V to power the LVDS transceiver. Do not select 5V as damage will occur to the LVDS transceiver.

The connectors on the following pages are shown in the same orientation as the picture above, unless otherwise stated.

Connector	Function
JP1	TX strobe selection
JP2	Cable power selection
JP3	MSL selection
J1	VIPER LCD output cable connector
J2	LVDS Hirose connector
J3	LVDS MDR connector

FPIF-LVDS-TX connectors

JP1 – TX strobe selection

This link selects the edge of the TX strobe.

If the jumper is fitted (default) then the TX Strobe shall be on the rising edge. If no jumper is fitted then the TX Strobe shall be on the falling edge.

Rising edge TX Strobe (Default)

Falling edge TX Strobe

JP2 – Cable power selection

This link provides 3.3V or 5V (default) to the J2 and J3 connectors respectively. Please refer to the pin descriptions of these connectors below for details.

If the FPIF-LVDS-TX is to be connected directly to an LVDS display then power for the display logic may be supplied to the display. If using long LVDS cables, it is advisable to use the CABLE_POWER signal as a control signal to enable power provided externally.

Backlight power for the display should always be provided externally.

If the FPIF-LVDS-TX is used in conjunction with the FPIF-LVDS-RX to extend the VIPER video up to 10 meters, fit the jumper to either position. Ensure that a jumper is fitted as the CABLE_POWER signal of the FPIF-LVDS-TX signals to the FPIF-LVDS-RX when to enable power to the display.

J2

J3(Default)

JP3 – MSL selection

If the FPIF-LVDS-TX is to be connected directly to an LVDS display via the Hirose connector J2, then this link selects the display's LVDS receiver input map. Fitting or not fitting a jumper to JP3 sets J2 pin 20 (MSL) to 3.3V or GND (default) respectively.

If the MDR connector J3 is used then jumper setting of JP3 has no effect.

Please consult the manual of your LVDS display for which setting to use for a National Semiconductor DS90C383 LVDS transceiver.

Open - GND (Default)

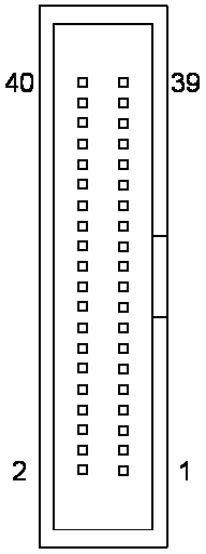
Closed - 3.3V

J1 – VIPER LCD cable connector

Connector: Oupiin 3215-40CSB/SN, 40-way, 1.27mm (0.05”) x 2.54mm (0.1”) straight-boxed header

Mating connector: Oupiin 1203-40GB/SN

Pin	Signal name	Pin	Signal name
40	HSYNC	39	CLOCK
38	GND	37	GND
36	DE	35	VSYNC
34	GND	33	GND
32	FPD 15	31	FPD 14
30	FPD 13	29	FPD 12
28	GND	27	GND
26	FPD 11	25	FPD 10
24	FPD 9	23	FPD 8
22	GND	21	GND
20	FPD 7	19	FPD 6
18	FPD 5	17	FPD 4
16	GND	15	GND
14	FPD 3	13	FPD 2
12	FPD 1	11	FPD 0
10	GND	9	GND
8	NC	7	NC
6	3VSAFE	5	NC
4	GND	3	GND
2	5VSAFE	1	PWRDWN#



J2 – LVDS Hirose connector

Connector: Hirose DF13-20DP-1.25V(55), 20-way, 1.27mm (0.05”) double row straight pin header

FPIF-LVDS-TX Hirose mating connector: Hirose DF13-20DS-1.25C

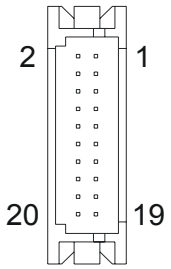
FPIF-LVDS-TX Hirose mating connector crimps: Hirose DF13-2630SCF

LVDS panel mating connector: Hirose DF14-20S-1.25C

LVDS panel mating connector crimps: Hirose DF14-2628SCF

Arcom recommended cable: Amphenol 165-2899-941 through to 165-2899-960

Pin	Signal name	Pin	Signal name
2	CABLE_POWER	1	CABLE_POWER
4	GND	3	GND
6	LVDS_D0+	5	LVDS_D0-
8	LVDS_D1-	7	GND
10	GND	9	LVDS_D1+
12	LVDS_D2+	11	LVDS_D2-
14	LVDS_CLK-	13	GND
16	GND	15	LVDS_CLK+
18	NC	17	NC
20	MSL	19	GND

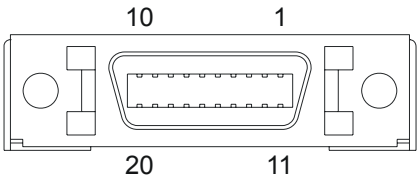


J3 – LVDS MDR connector

Connector: 3M 10220-55G3PL, 20-way, 1.27mm (0.05”) Board mount Through-Hole Right Angle Receptacle – Shielded

Mating cable: 3M 14520-EZAB-XXX-0EX, 3M™ Mini D Ribbon (MDR) Cable Assembly)

Pin	Signal name	Pin	Signal name
1	LVDS_D1+	11	LVDS_D2+
2	LVDS_D1-	12	LVDS_D2-
3	GND	13	GND
4	GND	14	GND
5	LVDS_CLK+	15	LVDS_D0+
6	LVDS_CLK-	16	LVDS_D0-
7	GND	17	NC
8	CABLE_POWER	18	NC
9	NC	19	NC
10	NC	20	NC



As viewed from the connector pins

FPIF-LVDS-RX details

The FPIF-LVDS-RX in combination with the FPIF-LVDS-TX allows the VIPER to drive a TFT or STN LCD flat panel display up to 10 meters away.

The connectors on the following pages are shown in the same orientation as the picture above, unless otherwise stated.

Connector	Function
JP1	LCD power selection
JP2	Backlight power selection
J1	LCD cable connector
J2	LVDS Hirose connector
J3	LVDS MDR connector
J4	Power connector

FPIF-LVDS-RX connectors

JP1 – LCD power selection

This link selects the voltage supply of the LCD panel.

Fit the jumper in position 3.3V (default) to supply 3.3V to the LCD panel, or in position 5V to supply 5V to the LCD panel.

3.3V LCD power (default)

5V LCD power

JP2 – Backlight power selection

This link selects the voltage supply of the LCD backlight.

Fit the jumper in position 5V (default) to supply 5V to the LCD backlight, or in position 12V to supply 12V to the LCD backlight.

5V backlight power (default)

12V backlight power

Must provide 5V to J4 to power the FPIF-LVDS-RX. The 3.3V supply is generated locally on the FPIF-LVDS-RX from the 5V supply.

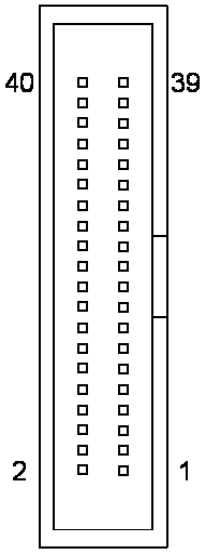
If the backlight requires 12V, then a 12V supply must be connected to J4.

J1 – VIPER LCD cable connector

Connector: Oupiin 3215-40CSB/SN, 40-way, 1.27mm (0.05”) x 2.54mm (0.1”) straight-boxed header

Mating connector: Oupiin 1203-40GB/SN

Pin	Signal name	Pin	Signal name
40	HSYNC	39	CLOCK
38	GND	37	GND
36	DE	35	VSYNC
34	GND	33	GND
32	FPD 15	31	FPD 14
30	FPD 13	29	FPD 12
28	GND	27	GND
26	FPD 11	25	FPD 10
24	FPD 9	23	FPD 8
22	GND	21	GND
20	FPD 7	19	FPD 6
18	FPD 5	17	FPD 4
16	GND	15	GND
14	FPD 3	13	FPD 2
12	FPD 1	11	FPD 0
10	GND	9	GND
8	NC	7	NC
6	LCDSAFE	5	NC
4	GND	3	GND
2	BLKSAFE	1	BLKEN#



J2 – LVDS Hirose connector

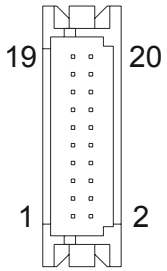
Connector: DF13-20DP-1.25V(55), 20-way, 1.27mm (0.05”) double row straight pin header

FPIF-LVDS-RX Hirose mating connector: Hirose DF13-20DS-1.25C

FPIF-LVDS-RX Hirose mating connector crimps: Hirose DF13-2630SCF

Arcom recommended cable: Amphenol 165-2899-941 through to 165-2899-960

Pin	Signal name	Pin	Signal name
19	GND	20	NC
17	NC	18	NC
15	LVDS_CLK+	16	GND
13	GND	14	LVDS_CLK-
11	LVDS_D2-	12	LVDS_D2+
9	LVDS_D1+	10	GND
7	GND	8	LVDS_D1-
5	LVDS_D0-	6	LVDS_D0+
3	GND	4	GND
1	LCD_EN	2	LCD_EN

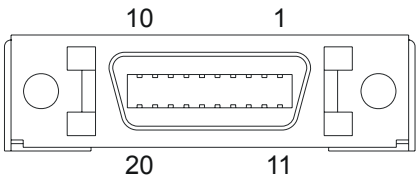


J3 – LVDS MDR connector

Connector: 3M 10220-55G3PL, 20-way, 1.27mm (0.05”) Board mount Through-Hole Right Angle Receptacle – Shielded

Mating cable: 3M 14520-EZAB-XXX-0EX, 3M™ Mini D Ribbon (MDR) Cable Assembly)

Pin	Signal name	Pin	Signal name
1	LVDS_D0-	11	LVDS_CLK-
2	LVDS_D0+	12	LVDS_CLK+
3	GND	13	GND
4	GND	14	GND
5	LVDS_D2-	15	LVDS_D1-
6	LVDS_D2+	16	LVDS_D1+
7	NC	17	NC
8	NC	18	NC
9	NC	19	LCD_EN
10	NC	20	GND



As viewed from the connector pins

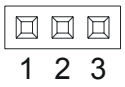
J4 – Power connector

Connector: FCI 76384-403LF, 3-way, 2.54mm (0.1”) Board mount Through-Hole Receptacle

Mating connector: FCI 65240-003LF

Mating connector crimps: FCI 76357-401LF

Pin	Signal name
1	5V
2	GND
3	12V



FPIF-CRT details

The FPIF-CRT allows the VIPER to drive a CRT Monitor or an analog LCD flat panel. Sync on green and composite sync monitors are not supported.

The connectors on the following pages are shown in the same orientation as the picture above, unless otherwise stated.

Connector	Function
J1	VIPER LCD cable connector
J2	CRT connector

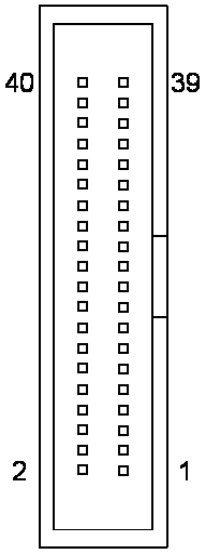
FPIF-CRT connectors

J1 – VIPER LCD cable connector

Connector: Oupiin 3215-40CSB/SN, 40-way, 1.27mm (0.05”) x 2.54mm (0.1”) straight-boxed header

Mating connector: Oupiin 1203-40GB/SN (available from Arcom on request)

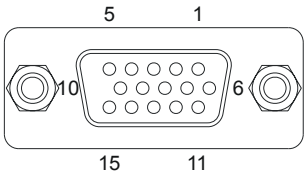
Pin	Signal name	Pin	Signal name
40	HSYNC	39	CLOCK
38	GND	37	GND
36	DE	35	VSYNC
34	GND	33	GND
32	FPD 15	31	FPD 14
30	FPD 13	29	FPD 12
28	GND	27	GND
26	FPD 11	25	FPD 10
24	FPD 9	23	FPD 8
22	GND	21	GND
20	FPD 7	19	FPD 6
18	FPD 5	17	FPD 4
16	GND	15	GND
14	FPD 3	13	FPD 2
12	FPD 1	11	FPD 0
10	GND	9	GND
8	NC	7	NC
6	NC	5	NC
4	GND	3	GND
2	5VSAFE	1	NC



J2 – CRT connector

Connector: Oupiin 7916-15FA/SN, 15-way, female, high density, right-angled D-Sub.

Pin	Signal name	Pin	Signal name	Pin	Signal name
1	RED	6	RED GND	11	NC
2	GREEN	7	GREEN GND	12	NC
3	BLUE	8	BLUE GND	13	HSYNC
4	NC	9	5V_VGASAFE	14	VSYNC
5	GND	10	SYNC GND	15	NC



(As viewed from the connector pins)

Audio

A National Semiconductor LM4549 AC'97 audio CODEC is used to support the audio features of the VIPER. Audio inputs supported by the LM4549 are stereo line in and a mono microphone input.

The LM4549 provides a stereo line out that can also be amplified by a National Semiconductor LM4880 250mW per channel power amplifier, suitable for driving an 8Ω load. The LM4549 AC'97 codec may be turned off if it is not required. See the section Audio power management, page 84, for details.

Connection to the VIPER audio features is via header PL6. See the table below for pin assignments and the section PL6 – Audio connector, page 91, for connector and mating connector details.

Function	Pin	Signal	Signal levels (max)	Frequency response (Hz)
Microphone	10	MIC input	1Vrms	20 – 20k
	9	MIC voltage reference output		
	7	Audio ground reference.		
Line in	1	Line input left	1Vrms	20 – 20k
	5	Line input right		
	3	Audio ground reference		
Line out	2	Line output left	1Vrms	20 – 20k
	6	Line output right		
	4	Audio ground reference		
Amp out	8	Amp output left	1.79V peak , 1.26Vrms (8Ω load) 223mW	20 – 20k
	11	Amp output right		
	12	Audio ground reference		

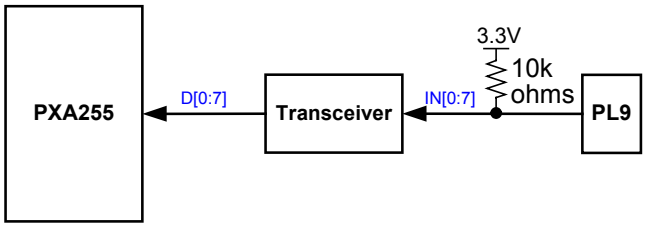
The left and right amp output signals are not AC coupled, these signals must be AC coupled with 100uF capacitors externally.

General purpose I/O

Eight general-purpose input lines and eight general-purpose output lines are provided on connector PL9.

To read from IN[0:7], read the least significant byte located at offset 0x500000 from CS5 (0x14000000) to sample the 8 inputs from PL9.

VIPER inputs	PXA255 data
IN0	D0
IN1	D1
IN2	D2
IN3	D3
IN4	D4
IN5	D5
IN6	D6
IN7	D7



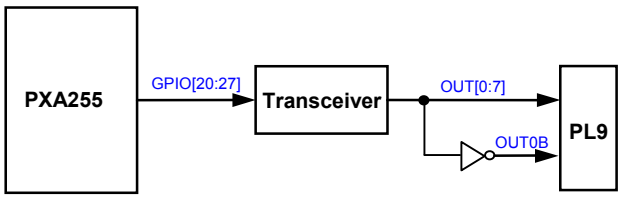
The PXA255 is not designed to interface to 8-bit peripherals, so when the 8-bits of data are read only the least significant byte from the word contains the data.

Data bus

Most Significant Byte								Least Significant Byte							
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Don't Care								IN Data							

To write to OUT[0:7], write to the following PXA255 processor GPIO lines to drive the outputs.

VIPER outputs	PXA255 GPIO
OUT0	GPIO20
OUT1	GPIO21
OUT2	GPIO22
OUT3	GPIO23
OUT4	GPIO24
OUT5	GPIO25
OUT6	GPIO26
OUT7	GPIO27



The PXA255 GPIO lines must be configured using the registers built into the device to ensure they function correctly. RedBoot configures GPIO20 – GPIO27 as outputs, and sets OUT0 to logic ‘0’, and OUT1 – 7 as logic ‘1’. Eboot cannot set these up as outputs as it only boots the Windows CE image. Once Windows CE is booted you can simply write to a mapped address. For an example of how to do this under Windows CE please see the Windows CE Technical Manual.

Please note:

- IN0-7 cannot be configured as outputs as they are hardwired as input-only by a buffer.
- OUT0-7 cannot be configured as inputs as they are hardwired as output-only by a buffer.
- OUT6-7 are not available if the VIPER is fitted with the TPM IC.

The GPIO lines are programmed using the GPCR0 and the GPSR0 to set the line to ‘0’ or ‘1’ respectively. The registers are 32-bit wide and bits 20-27 relate to GP20-27. To set one of the GP20-27 signals to a logic ‘1’ write a ‘1’ to the corresponding GPSR0 bit. To set one of the GP20-27 signals to a logic ‘0’ write a ‘1’ to the corresponding GPCR0 bit. To monitor the current state of a GP20-27 signal line read from GPLR0. A read-modify-write operation to GPLR0 will not change the state of the GP20-27 signal lines.

Register	Address
GPLR0	0x40E00000
GPSR0	0x40E00018
GPCR0	0x40E00024

The general-purpose inputs are 5V tolerant, and the outputs can sink and source up to 24mA @ 3.3V.

OUT0B is an inverted OUT0 signal, and is driven to 3.3V, which provides compatibility with the VIPER-UPS.

The following general purpose IO lines are used by the VIPER-UPS:

Function	IO
External Power Fail	IN0
Battery Low	IN1
UPS Power down	OUT0B

VIPER-I/O

The VIPER-I/O is a low cost add-on I/O module for the PXA255 board VIPER. The board provides a variety of I/O features without the additional costs of a full PC/104 interface. Please refer to the VIPER-I/O Technical Manual on the Development Kit CD.

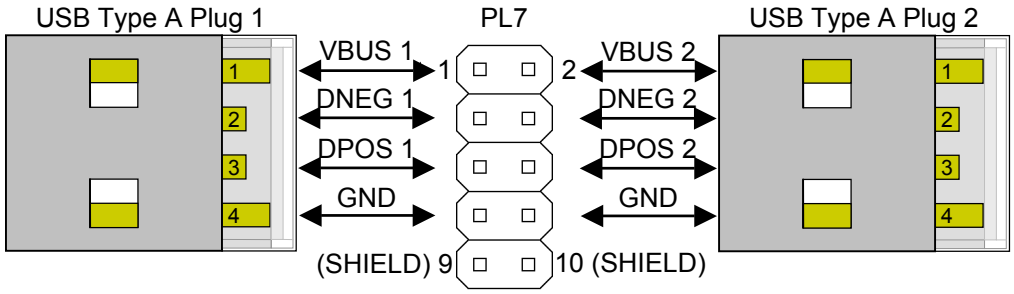
USB host interface

There are two USB interfaces on the VIPER. These comply with the Universal Serial Bus Specification Rev. 1.0a, supporting data transfer at full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s).

There are four signal lines associated with each USB channel:

- VBUS
- DPOS
- DNEG
- GND

Their arrangement is summarized in the following illustration:



A USB power control switch controls the power and protects against short-circuit conditions. See the section USB power management, page 83, for details of control.

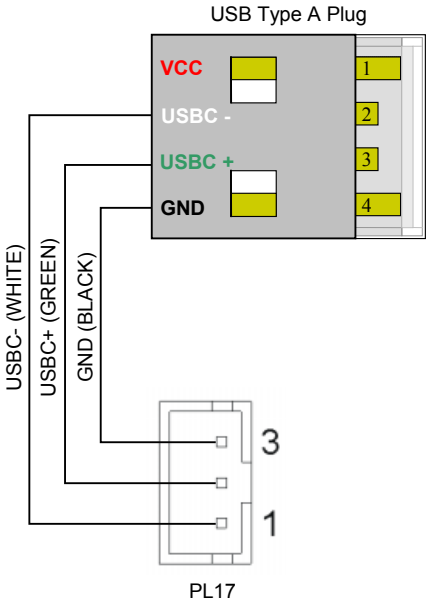
If the USB voltage is short-circuited, or more than 500mA is drawn from either supply, the switch turns off the power supply and automatically protects the device and board. The VBUS power supply is derived from the VIPER +5V supply.

If you require details for the USB bus, or would like to determine whether particular peripherals are available, see www.usb.org.

USB client interface

The VIPER provides one USB 1.1 client interface.

The connection between PL17 and a USB Type A connector is detailed in the following illustration:



10/100BaseTX Ethernet

An SMSC LAN91C111 Ethernet controller provides a single 10/100BaseTX interface. The device provides an embedded PHY and MAC, and complies with the IEEE802.3u 10/100BaseTX and IEEE 802.3x full-duplex flow control specifications. Configuration data and MAC information are stored in an external 93C46 EEPROM.

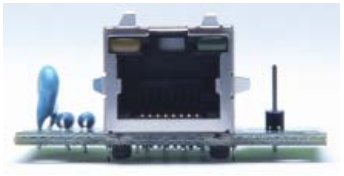
The 10/100base-T magnetics are located on the VIPER. Connection to the VIPER Ethernet port is via header PL1. See PL1 – 10/100BaseTX Ethernet connector, page 87, for pin assignment, connector, and mating connector details.

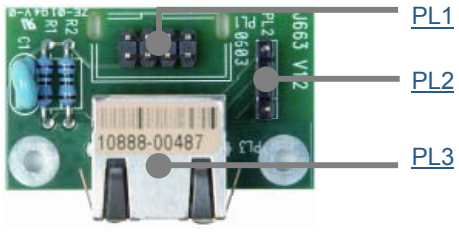
A second header PL2 provides the activity and link status LED signals. The output lines sink current when switched on therefore the anode of each LED should be connected to pins 1 and 3 of PL2 and the cathode to the appropriate status line.

The Link LED illuminates when a 10 or 100base-T link is made, and the activity LED illuminates when there is Tx or Rx activity.

Ethernet breakout board

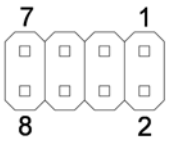
Arcom can provide an Ethernet breakout board with an RJ45 connector to interface to the VIPER Ethernet connectors PL1 and PL2. The Ethernet breakout board features brackets for panel mounting ease. The Ethernet breakout board allows easy connection between the VIPER and a 10/100base-T Ethernet connection:





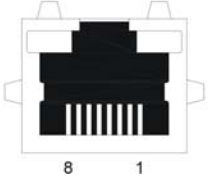
The connectors on the following pages are shown in the same orientation as the picture above.

Connector	Function
PL1	10/100BaseTX Ethernet signals
PL2	Ethernet LEDs
PL3	RJ45 connector



Ethernet breakout PL1

Ethernet breakout PL2



Ethernet breakout PL3

Ethernet signal mapping between VIPER and Ethernet breakout connectors

Ethernet breakout PL1 – 2x4-way header		Ethernet breakout PL3 - RJ45			VIPER PL1 – 10/100BaseTX Ethernet connector	
Pin	Signal name	Pin		Signal name	Pin	Signal name
1	Tx+	1		Tx+	1	Tx+
2	TX-	2		TX-	2	TX-
3	RX+	3		RX+	3	RX+
4	NC	4	}	Bob Smith Termination	4	NC
5	NC	5	}		5	NC
6	RX-	6		RX-	6	RX-
7	NC	7	}	Bob Smith Termination	7	NC
8	LANGND	8	}		8	LANGND

Ethernet LED signal mapping between VIPER and Ethernet breakout connectors

Ethernet breakout PL2 – 1x 4-way header		VIPER PL2 – Ethernet status LEDs connector	
Pin	Signal name	Pin	Signal name
1	LINK LED+	1	3.3V
2	LINK LED-	2	LINK (Green)
3	ACTIVITY LED+	3	3.3V
4	ACTIVITY LED-	4	ACTIVITY (Yellow)
		5	NC
		6	NC

Serial COMs ports

There are five high-speed, fully functionally compatible 16550 serial UARTs on the VIPER. Four of these channels can be used as standard RS232 serial interfaces, and the remaining one (COM5) can be configured as RS422 or RS485.

Port	Address	IRQ	FIFO depth RX / TX	Signals
COM1	0x40100000 – 0x40100023	Internal	64 / 64	RS232 Rx, Tx, CTS, RTS, RI, DSR, DCD, DTR
COM2	0x40200000 – 0x40200023	Internal	64 / 64	RS232 Rx, Tx, RTS, CTS
COM3	0x40700000 – 0x40700023	Internal	64 / 64	RS232 Rx, Tx
VL COM4	0x14300010 – 0x1430001F	GPIO4	128 / 128	RS232 Rx, Tx, CTS, RTS, RI, DSR, DCD, DTR
VL COM5	0x14300000 – 0x1430000F	GPIO3	128 / 128	RS422 / RS485 Tx, Rx

Please see the PXA255 Developer's Manual for details of internal interrupts.

COM1 – RS232 interface

Uses the full function UART in the PXA255 (FFUART). The port is buffered to RS232 levels with ±15kV ESD protection, and supports full handshaking and modem control signals. The maximum baud rate on this channel is 230.4kb/s (CPU max capability). A factory fit option configures COM1 as TTL Level signals to interface to a modem. Please contact Arcom for details. Contact details are provided in Appendix A – Contacting Arcom, page 101.

COM2 – RS232 interface

Uses the Bluetooth UART in the PXA255 (BTUART). The port is buffered to RS232 levels with ±15kV ESD protection, and supports full handshaking and modem control signals. The maximum baud rate on this channel is 921.6kb/s (CPU max capability).

COM3 – RS232 interface

Uses the Standard UART in the PXA255 (STUART). The port is buffered to RS232 levels with ±15kV ESD protection, and supports full handshaking and modem control signals. The maximum baud rate on this channel is 230.4kb/s (CPU max capability).

COM4 – RS232 interface

Supported on Channel 0 of an external Exar XR16C2850 with 128bytes of Tx and Rx FIFOs, and buffered to RS232 levels with ±15kV ESD protection. The maximum baud rate on this channel is 115.2kb/s. On special request this can be increased to 921.6kb/s. Please contact Arcom (see Appendix A – Contacting Arcom, page 101) for details.

COM5 – RS422/485 interface

Supported on Channel 1 of an external Exar XR16C2850 with 128bytes of Tx and Rx FIFOs, and buffered to RS422/485 levels with ±15kV ESD protection, to provide support for RS422 (default) and RS485 (jumper selectable) interfaces. The maximum baud rate on this channel is 115.2kb/s. On special request this can be increased to 921.6kb/s. Please contact Arcom (see Appendix A – Contacting Arcom, page 101) for details.

RS422

The RS422 interface provides full-duplex communication. The signals available are TXA, TXB, RXA, RXB, and Ground. The maximum cable length for an RS422 system is 4000ft (1200m) and supports 1 transmitter and up to 10 receivers.

To enable RS422 operation, LK6 and LK7 should be in position for RS422 full-duplex. LK4 and LK5 should be made if the board is at the end of the network. See RS485/422 configuration – LK4, LK5, LK6 and LK7, page 99, for details.

RS485

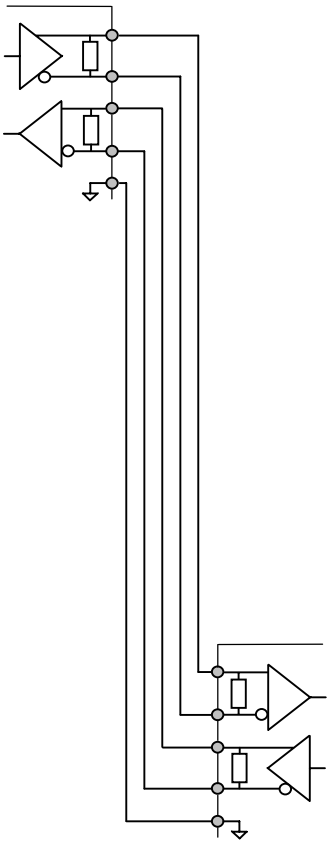
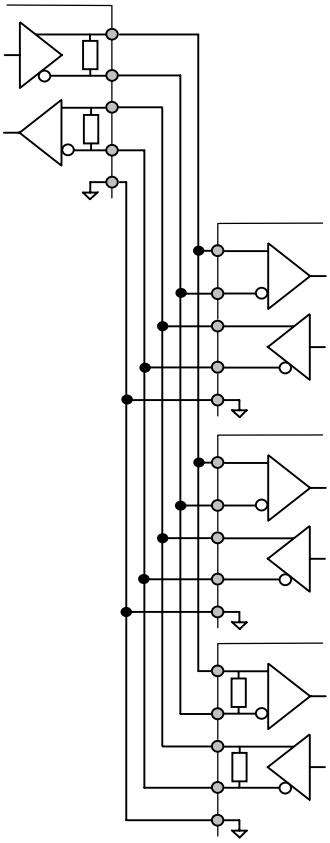
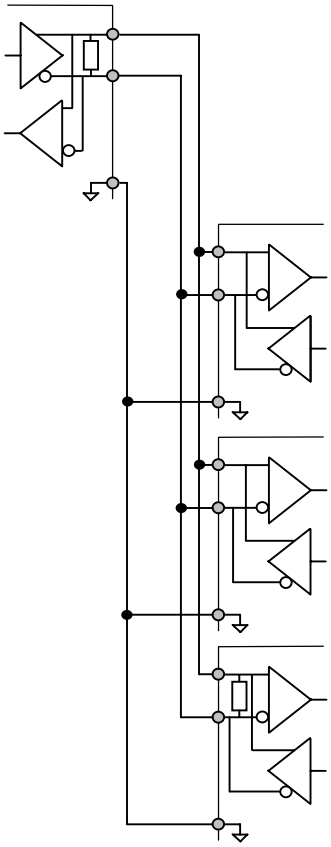
This is a half-duplex interface that provides combined TX and RX signals. PL4 pin 5 provides TXB/RXB and pin 6 provides TXA/RXA. A ground connection is also required for this interface. The maximum cable length for this interface is the same as RS422 (4000ft), but RS485 supports up to 32 transmitters and receivers on a single network. Only one transmitter should be switched on at a time.

The VIPER uses the RTS signal to control transmission. When this signal is at logic ‘1’ the driver is switched off and data can be received from other devices. When the RTS line is at logic ‘0’ the driver is on. Any data that is transmitted from the VIPER is automatically echoed back to the receiver. This enables the serial communications software to detect that all data has been sent and disable the transmitter when required. LK6 and LK7 should be in position RS485 half-duplex to enable the RS485 interface. See RS485/422 configuration – LK4, LK5, LK6 and LK7, page 99, for details. The UART used on the VIPER for COM5 has extended features including auto-RTS control for RS485. This forces the RTS signal to change state (and therefore the direction of the RS485 transceivers) when the last bit of a character has been sent onto the wire. Please refer to the XR16C2850 datasheet on the Development Kit CD.

LK4 and LK5 provide parallel line termination resistors and should be made if the VIPER is at the end of the network.

The RS422/485 cable shield MUST be connected between TITAN J1 pin 9 (GND) and the ground connection of the connecting equipment. Failure to do so can result in TITAN RS422/485 transceiver being permanently damaged.

Typical RS422 and RS485 connection

RS422 POINT-TO-POINT	RS422 MULTI-DROP	RS485 MULTI-DROP
		
Number of Wires 5 **Transmitters Enabled** always **Receivers Enabled** always **Duplex Mode** full **LK6** **B** **LK7** **B**	**Number of Wires** 5 **Transmitters Enabled** active RTS **Receivers Enabled** always **Duplex Mode** full **LK6** **B** **LK7** **B**	**Number of Wires** 3 **Transmitters Enabled** active RTS **Receivers Enabled** always **Duplex Mode** half **LK6** **A** **LK7** **A**

PC/104 interface

The VIPER PC/104 interface is emulated from the PXA255 PCMCIA interface to support 8/16 bit ISA bus style signals. As the interface is an emulation the VIPER does not support some PC/104 features. Please refer to the Unsupported PC/104 interface features, page 70, for specific details.

Add-on boards can be stacked via the PC/104 interface to enhance the functionality of the VIPER. Arcom has an extensive range of PC/104 compliant modules and these can be used to quickly add digital I/O, analog I/O, serial ports, video capture devices, PC card interfaces, etc.

Accessing the PC/104 interface

The ISA bus is based on the x86 architecture and is not normally associated with RISC processors. It is necessary to modify standard drivers to support any third party PC/104 modules.

Any PC/104 add-on board attached to the VIPER shall be available from the PC card memory space socket 1.

Address	Region name
0x3D000000 – 0x3FFFFFFF	Reserved
0x3C000000 – 0x3CFFFFFF	PC/104 memory space, 8 (write only) or 16-bit (16MB)
0x30000400 – 0x3BFFFFFF	Reserved
0x30000000 – 0x300003FF	PC/104 I/O space, 8 or 16-bit (1kB)

VIPER PC/104 interface details

The PC/104 bus signals are compatible with the ISA bus electrical timing definitions.

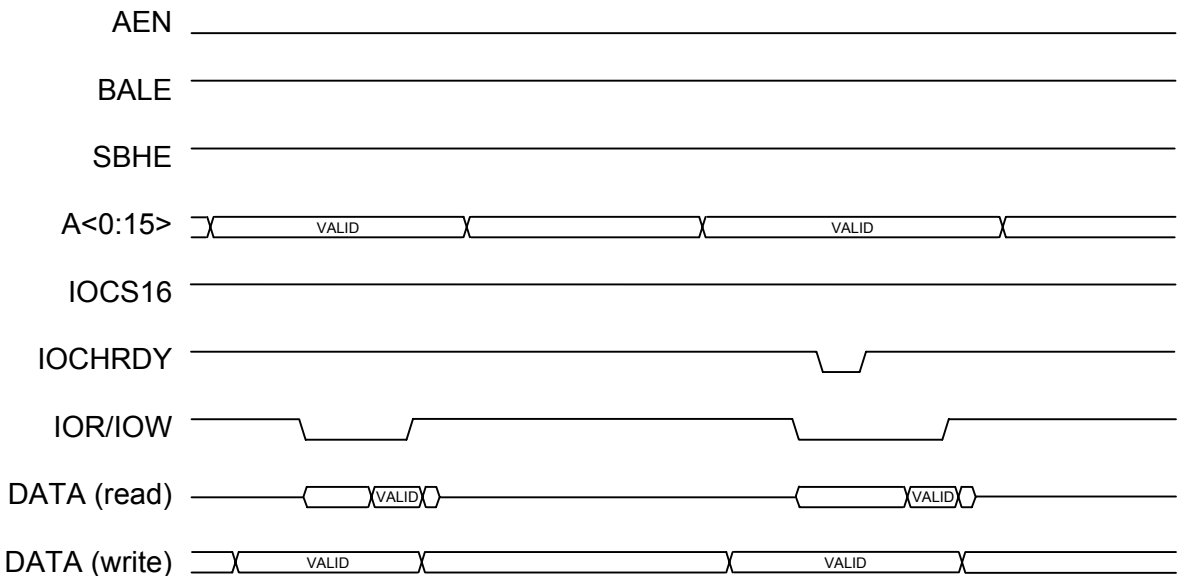
For details of PC/104 Interrupts please see PC/104 interrupts, page 30.

All signals (except interrupts) between the PXA255 and the PC/104 are buffered. The interrupts are connected and processed by CPLD. When the PC/104 bus is not in use all output signals, with the exception of the clock signals, are set to their inactive state.

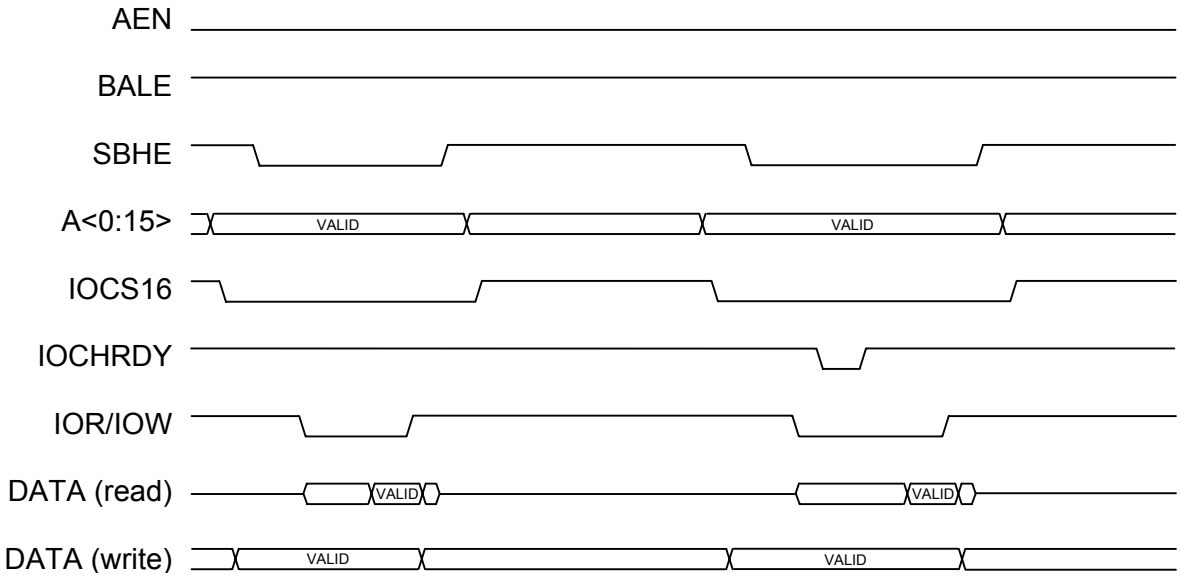
The VIPER provides +5V to a PC/104 add-on board via the PL11 and PL12 connectors. If a PC/104 add-on board requires a +12V supply, then +12V must be supplied to the VIPER power connector PL16 pin 4. If –12V or –5V are required, these must be supplied directly to the PC/104 add-on board.

The following diagrams show the activity of the VIPER PC/104 interface for 8 and 16-bit I/O and memory space accesses.

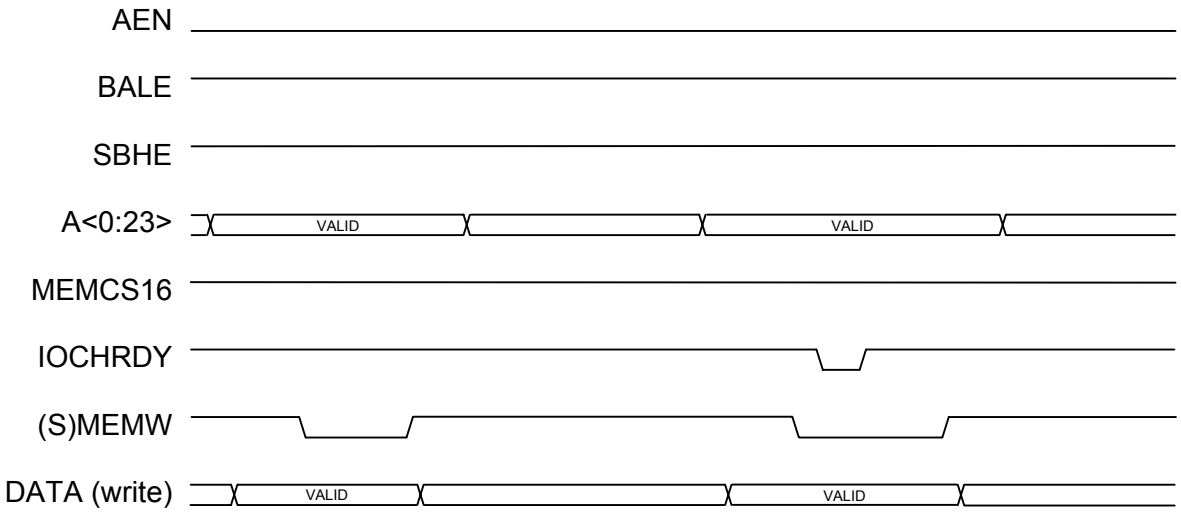
PC/104 8-bit I/O read/write access cycles



PC/104 16-bit I/O read/write access cycles

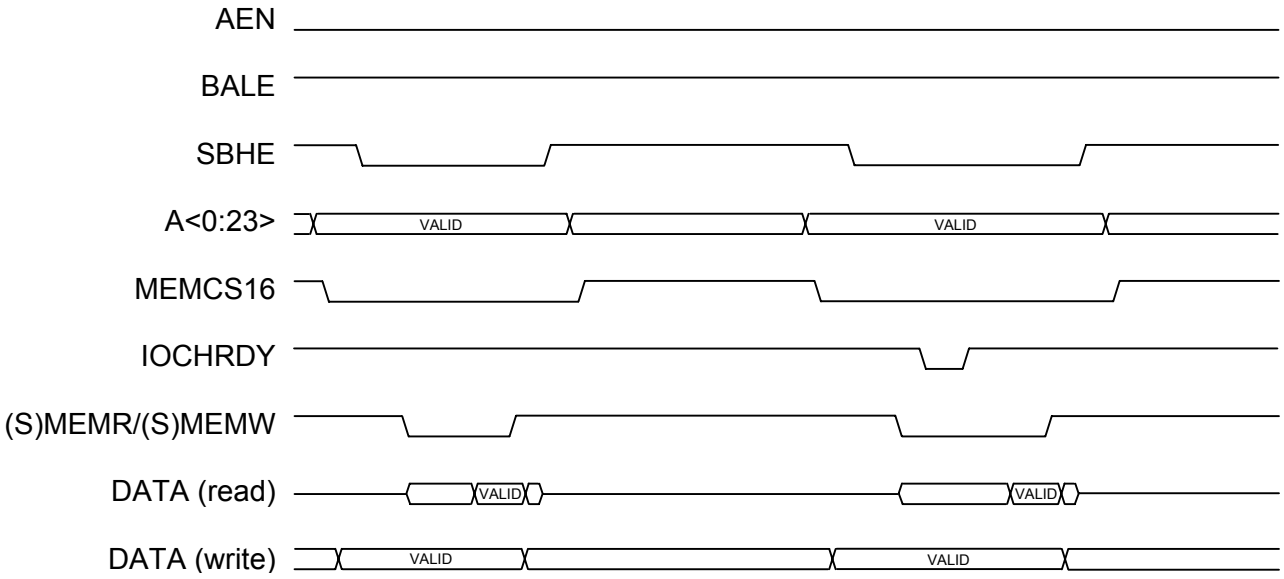


PC/104 8-bit memory write access cycle



8-bit memory read access cycles are not supported by the PXA255 PCMCIA controller for common memory space.

PC/104 16-bit memory read/write access cycles



Unsupported PC/104 interface features

The PC/104 bus features not supported by the VIPER are as follows:

- PC/104 IRQ9, IRQ14, and IRQ15 are not available under Windows CE as all interrupt sources are fully utilized. Therefore the PC104I2 register is not available.
- DMA is not supported on the VIPER's PC/104 interface. Therefore AEN is set to a constant logical zero.
- Bus Mastering is not supported on the VIPER's PC/104 interface. Therefore do not connect another VIPER or any other master add-on board to the VIPER PC/104 interface.
- Shared interrupts are not supported on the VIPER's PC/104 interface. Therefore do not connect more than one add-on board to the same interrupt signal line.
- BALE is set to a constant logical one as the address is valid over the entire bus cycle.
- The PXA255 PCMCIA memory controller does not support 8-bit memory read accesses for common memory space.

I²C

The PXA255 I²C interface is brought out to the COMs connector PL4, see PL4 – COMS ports, page 89, for connection details.

The I²C unit supports a fast mode operation of 400Kbits/s and a standard mode of 100Kbits/s.

Fast-mode devices are downward-compatible and can communicate with standard-mode devices in a 0 to 100Kbits/s I²C-bus system. As standard-mode devices, however, are not upward compatible, they should not be incorporated in a fast-mode I²C-bus system as they cannot follow the higher transfer rate and unpredictable states will occur.

The I²C unit does not support the hardware general call, 10-bit addressing, or CBUS compatibility.

Keep bus loads below 200pF.

TPM

The VIPER provides the option for an Atmel AT97SC3201 Trusted Platform Module (TPM), which provides full TCG/TCPA V1.1b compatibility. For further details please contact Arcom (see Appendix A – Contacting Arcom, page 101) for purchasing information.

When the TPM is fitted OUT6 and OUT7 from the general purpose I/O interface are not available.

JTAG and debug access

Debug access to the PXA255 processor is via the JTAG connector PL10. The Macraigor Wiggler and EPI Majic^{MX} probe have been used to debug the PXA255 processor on the VIPER. There are many other debug tools that can be interfaced to the VIPER for access to the JTAG Interface of the PXA255 processor.

The tables below detail the pins connections between the VIPER and Macraigor Wiggler or EPI Majic^{MX} debug tools. Of the Wiggler and Majic^{MX} debug tools the Wiggler provides the best low cost solution.

VIPER JTAG connections

	VIPER PL10		Debug tools pin names	
Pin	Name	Description	Majic^{MX}	Wiggler
1	VCC3	3.3V Supply pin to JTAG debug tool	VTRef, VSupply	Vref, VTarget
3	GND	Ground reference	GND	GND
4	nTRST	PXA255 JTAG interface reset	nTRST	nTRST
6	TDI	JTAG test data input to the PXA255	TDI	TDI
7	TDO	JTAG test data output from the PXA255	TDO	TDO
8	TMS	PXA255 JTAG test mode select	TMS	TMS
9	TCK	PXA255 JTAG test clock	TCK	TCK
10	SRST	System reset	nSRST	nSRST
2, 5	NC	No Connect	-	-
-	-	Not required on VIPER.	RTCLK	RTCK
-	-	Not required on VIPER	DBGREQ	DBGRQ
-	-	Not supported by VIPER	DBGACK	DBGACK

In order to access the PXA255 your JTAG software needs to know the details of the CPLD on the VIPER. The latest version of the ispMACH 4128C 100 Pin TQFP BSDL file can be found on the Lattice Semiconductor web site.

Power and power management

Power supplies

The VIPER is designed to operate from a single +5V ±5% (4.75V to +5.25V) supply. The power connector PL16 has a +12V connection defined, but is not required for the VIPER under normal operation. It can be used to supply +12V to the PC/104 stack if required. For details of the power connector please see the section PL16 – Power connector, page 95.

There are four onboard supply voltages derived from the +5V supply. These are +1.06 to +1.3V (microprocessor Core), +1.8V (CPLD Core) and two +3.3V. One +3.3V supply is dedicated for use with the CompactFLASH interface and +3.3V flat panels.

The +5V supply is monitored automatically on-board; if this supply falls below +4V the board is reset. When the power supply rises above this threshold voltage the board comes out of reset and reboots itself. The power supply monitor ensures that the board does not hang if the supply voltage fails at any point.

If a CompactFLASH and an LCD display are used, ensure the total current requirement on 3.3V does not exceed 900mA! Please check the datasheets of the devices you are using, as this supply is not protected!

Battery backup

An onboard Lithium-Ion non-rechargeable battery (CR2032) provides battery backup for the DS1338 RTC, SRAM, and optional TPM security feature when there is no +5V supply to the board. An external battery (CR2032 or similar) may also be fitted. To use an external battery see PL16 – Power connector, page 95 for connections.

The table below shows the typical and maximum current load on the external battery:

Device load on battery	Typical (µA)	Maximum (µA)
SRAM	0.2	2
DS1338 RTC with Clock Out Off / On	0.3 / 0.48	0.82/ 1.05
TPM (Optional)	2	4
Supply Supervisor	0.6	1
Total with RTC Clock Out Off	1.1 (3.1 with TPM)	3.82 (7.82 with TPM)
Total with RTC Clock Out On	1.28 (3.28 with TPM)	4.05 (8.05 with TPM)

An onboard Schottky diode drops 13mV from VBAT at 25°C. At -40°C this may increase to 170mV and at +85°C decrease below 10mV. The SRAM and DS1338 minimum voltages are 1.5V and 1.3V respectively. Reliable operation below these minimum voltages cannot be guaranteed.

The VIPER does not provide a battery charging circuit.

Power management

All VIPER power-down features and alteration of PXA255 operating frequency are fully supported under Embedded Linux and VxWorks. Windows CE currently provides no power management support.

To simplify the power consumption estimation of the VIPER, the following sections break down the process as follows:

- Processor current estimations, page 75.
- Power savings, page 77.
- External peripheral device power estimations, page 78.
- Power estimate examples, page 79.

The sections immediately following these detail the VIPER features that can be shutdown. See pages 81 to 84.

The section Processor current estimations, page 75, details current consumption of the VIPER for performance and power saving modes at different clock frequencies. Embedded Linux, Windows CE and VxWorks set up the PXA255 slightly differently:

- Embedded Linux and VxWorks are booted from Redboot, which sets up the PXA255 clock frequency to 100MHz (CCCR=0x121).
- Embedded Linux changes the Redboot setting to 400MHz in performance mode (CCCR=0x161).
- VxWorks makes no changes to the Redboot setting.
- Windows CE sets up the PXA255 clock frequency to 400MHz in power saving mode (CCCR=0x241).

The section Power savings, page 77, only apples to Linux and VxWorks power estimation calculations, as Windows CE currently does not provide any power management support. This section shows potential power savings for that can be achieved by shutting down sections of the VIPER that are not required.

The section External peripheral device power estimations, page 78, provides some examples of power consumption for various supported peripherals, such as LCD displays, CF, and USB devices, which may or may not be used for your application.

The section Power estimate examples, page 79, provides some examples to help you better understand how to use the information provided within the tables of the Processor current estimations, Power savings, and External peripheral device power estimations sections.

Processor current estimations

The current values in the tables below are referenced from running the VIPER at 400MHz in performance mode whilst the VIPER is idle.

The positive values (not shown in brackets) are the current saving by running the VIPER at slower frequencies or in power saving mode.

The negative values are the current increases that can be expected whilst the processor is near maximum activity load.

The values shown in brackets show the total current of the VIPER from the 5V supply before taking into account any power savings from shutting down VIPER features or including additional current for external peripherals.

Please refer to the relevant operating system Quickstart Manual to select an alternative operating frequency.

Processor	Vcore (V)	Current saving from 5V when processor core is in performance mode				
		400MHz CCCR=0x161	266MHz CCCR=0x143	200MHz CCCR=0x141	133MHz CCCR=0x123	Asleep
Active	1.29	-106mA ±20mA	-	-	-	-
Active	1.1	-	-47mA ±20mA	-	-	-
Active	1.06	-	-	-47mA ±20mA	-36mA ±20mA	-
Idle	1.29	0mA (334mA) [Linux default]	-	-	-	-
Idle	1.1	-	7mA (327mA)	-	-	-
Idle	1.06	-	-	7mA (327mA)	12mA (322mA)	-
Asleep	0	-	-	-	-	54mA (271mA)

Processor	Vcore (V)	Current saving from 5V when processor core is in power saving mode				
		400MHz CCCR=0x241	300MHz CCCR=0x321	200MHz CCCR=0x221	100MHz CCCR=0x121	Asleep
Active	1.29	-99mA ±20mA	-	-	-	-
Active	1.1	-	-46mA ±20mA	-	-	-
Active	1.06	-	-	-32mA ±20mA	-25mA ±20mA	-
Idle	1.29	9mA (325mA) [Win CE default]	-	-	-	-
Idle	1.1	-	19mA (316mA)	-	-	-
Idle	1.06	-	-	19mA (315mA)	29mA (308mA) [Redboot / VxWorks default]	-
Asleep	0	-	-	-	-	54mA (271mA)

Current figures when the microprocessor is active were taken with the following load conditions: calculating checksums of two files (first file: 1.1MB and second file: 0.5MB), and copying two 256kB files.

When the microprocessor is asleep the PC/104 and AC97' Codec clocks are shutdown.

Power savings

Use the table below to estimate power savings that can be achieved by shutting down features of the VIPER, or putting the VIPER to sleep.

					Power saving mode			Performance mode		
CPU	Ethernet	USB VL	Audio VL	Serial	Current saving ±3mA	Total current ±3mA	Total power ±15mW	Current saving ±3mA	Total current ±3mA	Total power ±15mW
-	-	-	-	-	0mA	325mA	1625mW	0mA	334mA	1670mW
-	-	-	-	Sleep	25mA	300mA	1500mW	25mA	309mA	1545mW
-	-	-	Sleep	-	38mA	287mA	1435mW	38mA	296mA	1480mW
-	-	-	Sleep	Sleep	64mA	261mA	1305mW	64mA	270mA	1350mW
-	-	Sleep	-	-	37mA	288mA	1440mW	37mA	297mA	1485mW
-	-	Sleep	-	Sleep	62mA	263mA	1315mW	62mA	272mA	1360mW
-	-	Sleep	Sleep	-	77mA	248mA	1240mW	77mA	257mA	1285mW
-	-	Sleep	Sleep	Sleep	100mA	225mA	1125mW	100mA	234mA	1170mW
-	Sleep	-	-	-	108mA	217mA	1085mW	108mA	226mA	1130mW
-	Sleep	-	-	Sleep	131mA	194mA	970mW	131mA	203mA	1015mW
-	Sleep	-	Sleep	-	146mA	179mA	895mW	146mA	188mA	940mW
-	Sleep	-	Sleep	Sleep	172mA	155mA	775mW	172mA	162mA	810mW
-	Sleep	Sleep	-	-	143mA	182mA	910mW	143mA	191mA	955mW
-	Sleep	Sleep	-	Sleep	167mA	158mA	790mW	167mA	167mA	835mW
-	Sleep	Sleep	Sleep	-	181mA	144mA	720mW	181mA	153mA	765mW
-	Sleep	Sleep	Sleep	Sleep	205mA	120mA	600mW	205mA	129mA	645mW
Sleep	Sleep	Sleep	Sleep	Sleep	276mA	49mA	245mW	285mA	49mA	245mW

External peripheral device power estimations

Take into account any external peripherals for your application, such as:

- USB devices: keyboard, memory stick, and mouse.
- CompactFLASH socket: CompactFLASH memory, or Microdrive.
- Flat panel display: TFT logic + backlight, STN logic + backlight + bias voltage.

The table below gives examples of addition current/power from external peripheral devices:

Device	Part number	Condition	Additional current	Additional power
32MB Sandisk CompactFLASH	SDCFB-32-101-80	Inserted, (no access)	1mA	5mW
		Reading constantly	48mA	240mW
64MB FlashDio™ USB memory stick	FDU100A	Inserted, (no access)	75mA	375mW
		Reading constantly	121mA	605mW
NEC 5.5” LCD + Inverter (as used with VIPER-ICE)	NL3224BC35-20 + 65PW31	LCD and backlight on	650mA	3250mW
		LCD on and backlight off	291mA	1455mW

For devices using the 3.3V supply from the CompactFLASH socket and FPD logic supply, use 92% as the regulator efficiency.

Power estimate examples

Example 1: VIPER [Linux] asleep (microprocessor in sleep mode and every power saving option enabled)

In this case, the power consumed by the respective categories is:

- VIPER current (Linux default) = 334mA ±3mA.
- Power saving = 285mA (all power saving options enabled).
- External peripheral current = 0mA.

Therefore, the estimated VIPER current is:

334mA ±3mA - 285mA + 0mA
= 49mA ±3mA (245mW ±15mW).

Example 2: VIPER [Linux] at 200MHz in performance mode + LCD with backlight on

In this case, the power consumed by the respective categories is:

- VIPER current while idle = 334mA ±3mA - 7mA = 327mA ±3mA.
  VIPER current while active = 334mA + 47mA ±20mA = 381mA ±20mA.
- Power saving = 0mA.
- External peripheral current = 650mA (LCD).

Therefore, the estimated VIPER current while idle (min) is:

327mA ±3mA + 650mA
= 977mA, ±3mA (4885mW, ±15mW).

and the estimated VIPER current while active (max) is:

381mA ±20mA + 650mA
= 1031mA, ±20mA (5155mW, ±100mW).

Example 3: VIPER [Windows CE] at 400MHz in power saving mode + LCD with backlight on + 64MB FlashDio™ USB memory stick

In this case, the power consumed by the respective categories is:

- VIPER current (Windows CE default) while idle = 334mA ±3mA - 9mA
  = 325mA ±3mA.
  VIPER current (Windows CE default) while active = 334mA + 99mA ±20mA
  = 433mA ±20mA.

- Power saving = 0mA.

- External peripheral current (USB memory stick quiescent) = 650mA (LCD) + 75mA
  = 725mA.
  External peripheral current (USB memory stick read) = 650mA (LCD) + 121mA
  = 771mA

Therefore, the estimated VIPER current while idle (min) is:

325mA ±3mA + 725mA
= 1050mA, ±3mA (5250mW, ±15mW).

and the estimated VIPER current while active and reading from USB memory stick (max) is:

433mA ±20mA + 771mA
= 1204mA, ±20mA (6020mW, ±100mW) .

Processor power management

The power manager in the PXA255 offers the ability to disable the clocks to the different internal peripherals. By default, all clocks are enabled after reset. To reduce power consumption disable the clocks for any unused peripherals.

The clock speed of the processor core, PXbus (the internal bus connecting the microprocessor core and the other blocks of the PXA255), LCD, and SDRAM can also be changed to achieve a balance between performance and power consumption. For more details on the internal power manager please see the PXA255 Developer's Manual on the Development Kit CD.

To adjust the core voltage, write the values shown in the following table to the LTC1659 DAC. When changing the core voltage it is important to ensure that the internal CPU clock is set to the correct voltage range. The CPU core supply must be set to a defined range for a particular clock. Please refer to the LTC1659 datasheet, Clocks and Power Manager section in the PXA255 Applications Processors Developer's Manual and Power Consumption Specifications section in the PXA255 Processor Electrical, Mechanical, and Thermal Specification on the Development Kit CD.

DAC Data Hex value	CPU core voltage	Comment
0x000	1.65V	Not recommended to set the VCORE above 1.3V as the power consumption will increase for no performance benefit.
0x325	1.29V	Typical VCORE for peak voltage range at 400MHz operation. Maximum VCORE for medium voltage range at 200MHz operation.
0xDE5	1.1V	Typical VCORE for high voltage range at 300MHz operation.
0xFFF	1.06V	Typical VCORE for low voltage and medium voltage range, suitable for 100MHz to 200MHz operation.

When the microprocessor is in sleep mode, the CPU core voltage is shutdown.

When changing between CPU core voltages it is important to adjust the DAC Data in steps of no greater than 0x100 at a time.

To communicate with the VCORE DAC, use the following pins to emulate the LTC1659 interface:

GPIO	LTC1659 DAC pin function
GPIO6	Data
GPIO11	Clock
GPIO19	Chip Select

Before putting the PXA255 into sleep mode, ensure the R_DIS bit in the ICR register is set to '1'. The PXA255 is not designed to interface to 8-bit peripherals, so only the least significant byte from the word contains the data.

Interrupt configuration and reset register

Byte lane	Most Significant Byte								Least Significant Byte							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	-	-	-	-	-	-	-	-	-	-	-	-	CF_RST	R_DIS	AUTO_CLR	RETRIG
Reset	X	X	X	X	X	X	X	X	0	0	0	0	0	0	0	0
R/W	-	-	-	-	-	-	-	-	R				R/W			
Address	0x14100002															

ICR bit functions

Bit	Name	Value	Function
0	RETRIG	0	No interrupt retrigger (embedded Linux/VxWorks)
		1	Interrupt retrigger (Windows CE)
1	AUTO_CLR	0	No auto clear interrupt / Toggle GPIO1 on new interrupt (embedded Linux and VxWorks).
		1	Auto clear interrupt / pulse low for 1.12µS on GPIO1 on new interrupt from a new interrupt source (Windows CE).
2	R_DIS	0	Board reset normal
		1	Board reset disable (Set before entering CPU sleep)
3	CF_RST	0	CompactFlash reset controlled by board reset
		1	Reset CompactFlash
4 - 7	-	X	No function

UART power management

COM4 and COM5 are generated from an external Exar XR16C2850 DUART. This device supports a sleep mode. By enabling this feature the DUART enters sleep mode when there are no interrupts pending. Please see the XR16C2850 datasheet on the Development Kit CD for information on enabling the sleep mode.

GPIO12 on the PXA255 can be used to power down the RS232 transceivers on COM1, 2, 3, and 4. The following table shows the affect of GPIO12 on the RS232 transceivers:

GPIO12	Operation status	Transmitters	Receivers
0	Normal operation	Active	Active
1	Shutdown	High-Z	High-Z

Placing the XR16C2850 and the RS232 transceivers into low power mode can reduce the power consumption of the VIPER up to 25mA ±3mA (125mW ±15mW).

CompactFLASH power management

The power supply to the CompactFLASH interface is controlled via software, and supports hot swap card insertion and CompactFLASH power down states. GPIO82 on the PXA255 is used to control the power supply. Setting this line to logic ‘0’ switches off power to the CompactFLASH interface.

Ethernet power management

The network interface supports a power down mode, which shuts down the internal MAC and PHY blocks of the network controller. Placing the controller into low power mode can reduce the power consumption of the VIPER by up to108mA ±3mA (540mW ±15mW). To power down the PHY write ‘1’ to the power down bit in the MII PHY Register 0, Control Register. To power down the MAC write ‘1’ to the EPH PowerEN bit in the Bank 1, Configuration Register. See the LAN91C111 datasheet contained on the Development Kit CD for further details.

USB power management

The USB Host controller supports a USB suspend state. Placing the controller into the USB suspend state can reduce the power consumption of the VIPER by up to 37mA ±3mA (185mW ±15mW). To suspend the USB, the software must write to the relevant bits in the HcControl Register (81h). Please see the ISP1160 datasheet contained on the Development Kit CD.

To wake the USB Host Controller from suspend, pulse GPIO13 high.

Audio power management

The audio interface supports the AC'97 low power modes. Shutting down the digital and analog interfaces can reduce consumption by up to 38mA ±3mA (190mW ±15mW).

To shut down the AC'97 Codec, the software must write to the relevant bits in the Powerdown Control / Status Register (26h). Please see the LM4549 datasheet contained on the Development Kit CD.

TPM

If the VIPER has the TPM option the VIPER consumes a further 3.5mA (17.5mW) while the TPM IC is idle, and 17mA (85mW) while the TPM IC is operating. This device cannot be shutdown.

Wake up events

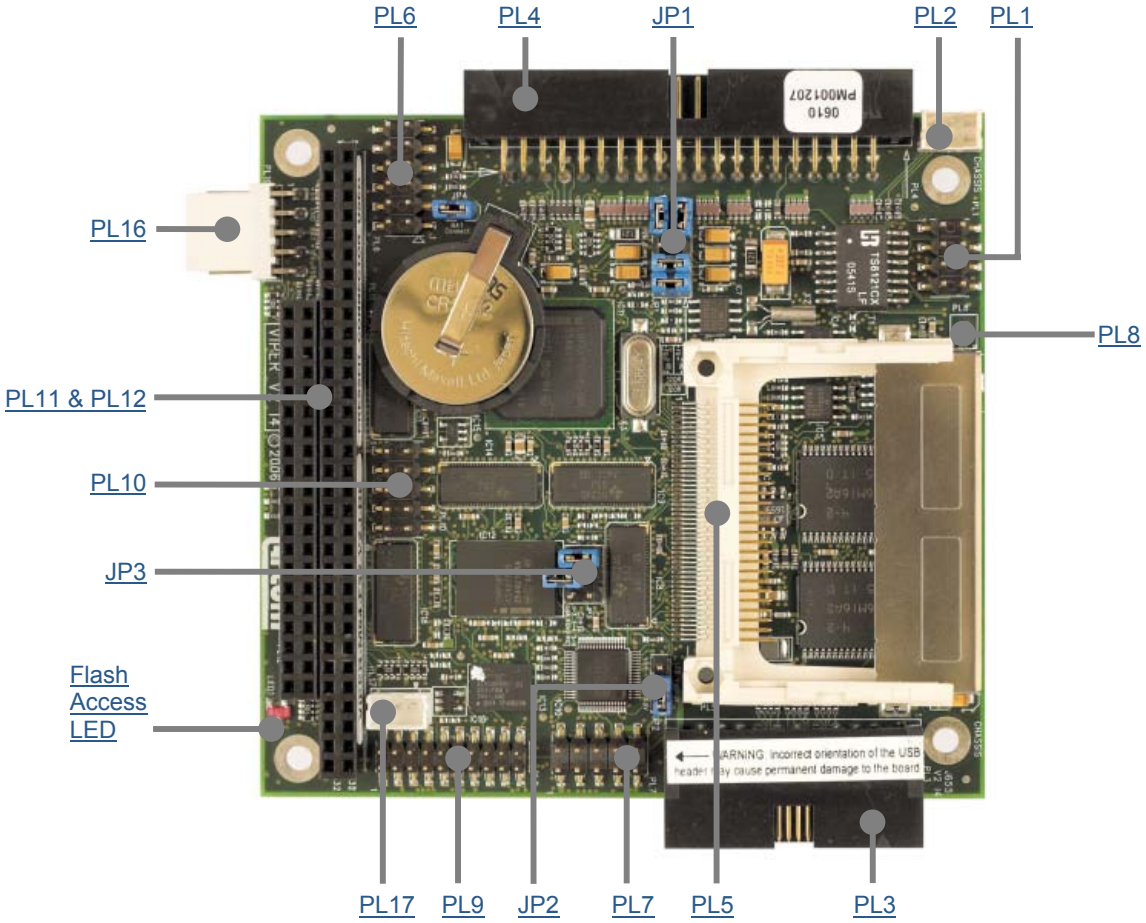
When the PXA255 processor is placed into sleep mode, two sources can be used to wake the processor.

Source	GPIO
USER_CONFIG1	GPIO7
RTC Alarm	Internal

See section 3.5 in the PXA255 Applications Processor Developers Manual, included in the Development Kit CD.

Connectors, LEDs, and jumpers

The following diagram shows the location of the connectors, LEDs, and jumpers on the VIPER:



The connectors on the following pages are shown in the same orientation as the picture above, unless otherwise stated.

Connectors

There are 13 connectors on the VIPER for accessing external devices:

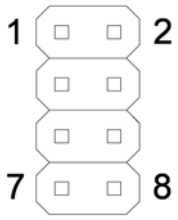
	Connector	Function	Connector details in section...
	PL1	10/100BaseTX Ethernet interface	PL1 – 10/100BaseTX Ethernet connector, page 87
	PL2	Ethernet controller status LEDs	PL2 – Ethernet status LEDs connector, page 87
	PL3	LCD panel interface	PL3 – LCD connector, page 88
	PL4	Serial ports	PL4 – COMS ports, page 89
	PL5	CompactFLASH type I/II	PL5 – CompactFLASH connector, page 90
VL	PL6	Audio	PL6 – Audio connector, page 91
VL	PL7	USB	PL7 – USB connector, page 91
VL	PL8	TPM Tamper Detect	PL8 – TPM Tamper connector, page 92
	PL9	GPIO	PL9 – GPIO connector, page 92
	PL10	JTAG	PL10 – JTAG connector, page 93
VL	PL11	64-way PC/104 expansion	PL11 & PL12 – PC/104 connectors, page 94
VL	PL12	40-way PC/104 expansion	PL11 & PL12 – PC/104 connectors, page 94
	PL16	Power / battery / external reset	PL16 – Power connector, page 95
	PL17	USB client	PL17 – USB client connector, page 95
VL	JP1	RS485/422 configuration jumpers	JP1 – RS485/422 configuration jumpers, page 96
	JP2	LCD voltage select jumper	JP2 – LCD voltage select jumper, page 96
	JP3	User configuration and reset jumper	JP3 – User configuration and reset jumper, page 96
	JP4	Battery jumper	JP4 – Battery jumper, page 96

PL1 – 10/100BaseTX Ethernet connector

Connector: Oupiin 2015-2X4GD/SN, 8-way, 2.54mm (0.1”) x 2.54mm (0.1”) dual row header

Mating connector: FCI 71600-008LF

Pin	Signal name	Pin	Signal name
1	TX+	2	TX-
3	RX+	4	NC
5	NC	6	RX-
7	NC	8	LANGND



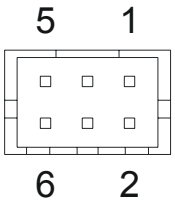
PL2 – Ethernet status LEDs connector

Connector: Neltron 2417SJ-06-PHD, 6-way, 2mm (0.079”) x 2mm (0.079”) pin housing

Mating connector: Neltron 2418HJ-06-PHD

Mating connector crimps (x4): Neltron 2418TJ-PHD

Pin	Signal name	Pin	Signal name
1	3.3V	2	Link
3	3.3V	4	Activity
5	NC	6	NC

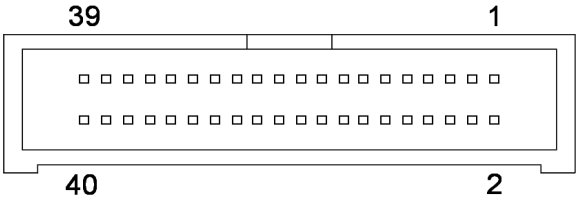


PL3 – LCD connector

Connector: Oupiin 3214-40C00RBA/SN, 40-way, 1.27mm (0.05”) x 2.54mm (0.1”) right angled boxed header

Mating connector: Oupiin 1203-40GB/SN

Pin	Signal name	Pin	Signal name
1	BLKEN#	2	BLKSAFE
3	GND	4	GND
5	NEGBIAS	6	LCDSAFE
7	GPIO16/PWM0	8	POSBIAS
9	GND	10	GND
11	FPD0	12	FPD1
13	FPD2	14	FPD3
15	GND	16	GND
17	FPD4	18	FPD5
19	FPD6	20	FPD7
21	GND	22	GND
23	FPD8	24	FPD9
25	FPD10	26	FPD11
27	GND	28	GND
29	FPD12	30	FPD13
31	FPD14	32	FPD15
33	GND	34	GND
35	FCLK / VSYNC	36	BIAS / DE
37	GND	38	GND
39	PCLK / CLOCK	40	LCLK / HSYNC



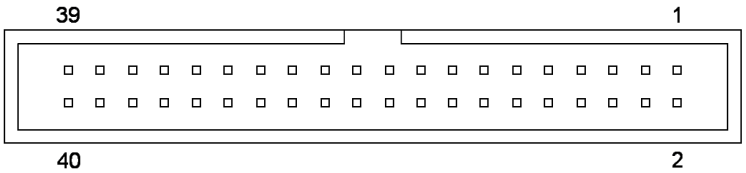
As viewed from the connector pins

PL4 – COMS ports

Connector: Oupiin 3012-40GRB/SN, 40-way, 2.54mm (0.1”) x 2.54mm (0.1”) dual row IDC boxed header

Mating connector: FCI 71600-040LF

	Pin	Signal name	Pin	Signal name	
	1	SCL (I^2C)	2	SDA (I^2C)	I^2C
	3	GND (I^2C)	4	3.3V (I^2C)	
VL	5	TX5+ (RS422) (TX5+/RX5+ RS485)	6	TX5- (RS422) (TX5-/RX5- RS485)	COM5
VL	7	RX5+ (RS422)	8	RX5- (RS422)	COM5
	9	GND	10	GND	COM3
	11	TX3	12	RX3	COM3
	13	RX2	14	RTS2	COM2
	15	TX2	16	CTS2	COM2
	17	GND	18	GND	
	19	GND	20	NC	
VL	21	DCD4	22	DSR4	COM5
VL	23	RX4	24	RTS4	COM5
VL	25	TX4	26	CTS4	COM5
VL	27	DTR4	28	RI4	COM5
VL	29	GND	30	NC	COM5
	31	DCD1	32	DSR1	COM1
	33	RX1	34	RTS1	COM1
	35	TX1	36	CTS1	COM1
	37	DTR1	38	RI1	COM1
	39	GND	40	NC	

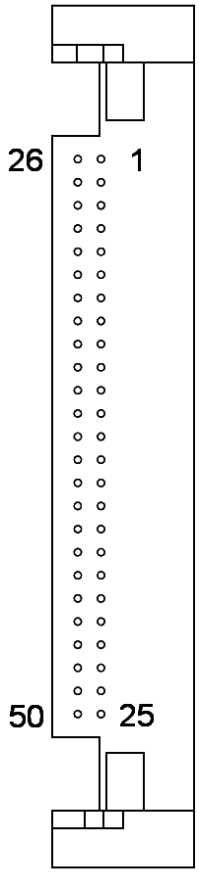


As viewed from the connector pins

PL5 – CompactFLASH connector

Connector: 3M N7E50-N516RB-50, 50-way CompactFLASH Type II Connector

Pin	Signal name	Pin	Signal name
26	/CD1	1	GND
27	D11	2	D03
28	D12	3	D04
29	D13	4	D05
30	D14	5	D06
31	D15	6	D07
32	/CE2	7	/CE1
33	/VS1 (GND)	8	A10
34	/IORD	9	/OE
35	/IOWR	10	A09
36	/WE	11	A08
37	RDY/BSY	12	A07
38	+3.3V	13	+3.3V
39	CSEL (GND)	14	A06
40	N/C	15	A05
41	/RESET	16	A04
42	WAIT	17	A03
43	/INPACK (NU)	18	A02
44	/REG	19	A01
45	N/C	20	A00
46	N/C	21	D00
47	D08	22	D01
48	D09	23	D02
49	D10	24	/IOCS16
50	GND	25	/CD2

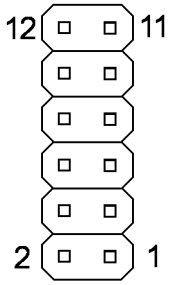


PL6 – Audio connector

Connector: Oupiin 2015-2X6GDB/SN, 12-way, 2.54mm (0.1”) x 2.54mm (0.1”) dual row header

Mating connector: FCI 71600-014LF (with pins 13 and 14 blanked off)

Pin	Signal name	Pin	Signal name
1	LEFT IN	2	LEFT OUT
3	GND	4	GND
5	RIGHT IN	6	RIGHT OUT
7	GND	8	AMP LEFT OUT
9	MIC VREF OUT	10	MIC IN
11	AMP RIGHT OUT	12	GND

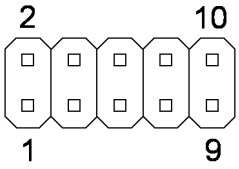


PL7 – USB connector

Connector: Oupiin 2011-2x5GSB/SN, 10-way, 2.54mm (0.1”) x 2.54mm (0.1”) dual row header

Mating connector: FCI 71600-010LF

Pin	Signal name	Pin	Signal name
1	VBUS-1	2	VBUS-2
3	DNEG-1	4	DNEG-2
5	DPOS-1	6	DPOS-2
7	GND	8	GND
9	SHIELD	10	SHIELD



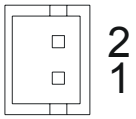
PL8 – TPM Tamper detect connector (optional)

Connector: JST B2B-ZR(LF)(SN), 2-way, single row, 1.5 mm (0.06”) Shrouded Header

Mating housing: JST ZHR-2

Mating housing crimps: JST SZH-002T-P0.5

Pin	Signal name	Pin	Signal name
1	VCC_BACKUP	2	TPM_TAMPER_DETECT



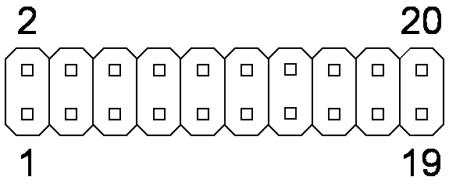
PL9 – GPIO connector

Connector: Oupiin 2115-2X10GDN/SN, 20-way, 2mm (0.079”) x 2mm (0.079”) dual row header

Mating connector: FCI 69307-020LF

Mating connector crimps (x20): FCI 77138-001LF

Pin	Signal name	Pin	Signal name
1	+5V	2	+5V
3	IN0	4	IN1
5	IN2	6	IN3
7	IN4	8	IN5
9	IN6	10	IN7
11	OUT0	12	GND
13	OUT0_ INVERTED	14	OUT1
15	OUT2	16	OUT3
17	OUT4	18	OUT5
19	OUT6	20	OUT7

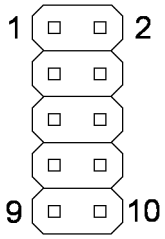


PL10 – JTAG connector

Connector: Oupiin 2011-2x5GSB/SN, 10-way, 2.54mm (0.1”) x 2.54mm (0.1”) dual row header

Mating connector: FCI 71600-010LF

Pin	Signal name	Pin	Signal name
1	VCC3	2	NC
3	GND	4	nTRST
5	NC	6	TDI
7	TDO	8	TMS
9	TCLK	10	SRST

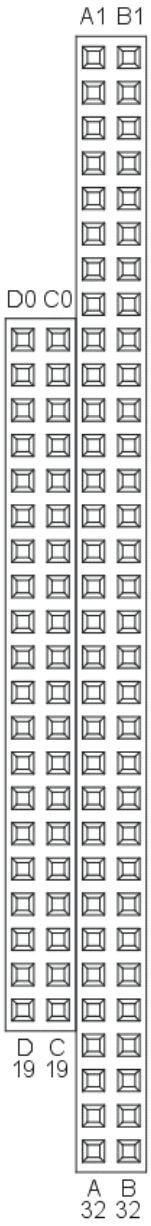


PL11 & PL12 – PC/104 connectors

Connectors:

- Astron 25-1201-232-2G-R, 64-way, 2.54mm (0.1”) x 2.54mm (0.1”) Stackthrough PC/104 compatible connector (row A & B)
- Astron 25-1201-220-2G-R, 40-way, 2.54mm (0.1”) x 2.54mm (0.1”) Stackthrough PC/104 compatible connector (row C & D)

	PL12		PL11		
Pin	Row D	Row C	Pin	Row A	Row B
			1	/IOCHCK	GND
			2	D7	RSTDRV
			3	D6	+5V
			4	D5	IRQ9
			5	D4	NC
			6	D3	NU (DRQ2)
			7	D2	NC
			8	D1	NC
0	GND	GND	9	D0	+12V
1	/MEMCS16	/SBHE	10	IOCHRDY	KEY
2	/IOCS16	LA23	11	AEN	/SMEMW
3	IRQ10	LA22	12	A19	/SMEMR
4	IRQ11	LA21	13	A18	/IOW
5	IRQ12	LA20	14	A17	/IOR
6	IRQ15	LA19	15	A16	NU (DACK3)
7	IRQ14	LA18	16	A15	NU (DRQ3)
8	NU (DACK0)	LA17	17	A14	NU (DACK1)
9	NU (DRQ0)	/MEMR	18	A13	NU (DRQ1)
10	NU (DACK5)	/MEMW	19	A12	NU (REFSH)
11	NU (DRQ5)	D8	20	A11	8MHz Clk
12	NU (DACK6)	D9	21	A10	IRQ7
13	NU (DRQ6)	D10	22	A9	IRQ6
14	NU (DACK7)	D11	23	A8	IRQ5
15	NU (DRQ7)	D12	24	A7	IRQ4
16	+5V	D13	25	A6	IRQ3
17	NC (Master)	D14	26	A5	NU (DACK2)
18	GND	D15	27	A4	NU (TC)
19	GND	KEY	28	A3	BALE
			29	A2	+5V
			30	A1	OSC
			31	A0	GND
			32	GND	GND

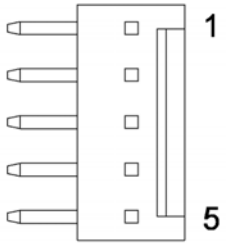


PL16 – Power connector

Connector: Molex 22-05-7058, 5-way, 2.54mm (0.1") Pitch KK® Header - Right Angle Friction Lock 7395 series connector

Mating connector: Molex 22-01-2055, 5-way, 2.54mm (0.1") Pitch KK® Crimp Terminal Housing 2695 series connector

Pin	Signal name
1	+5V
2	GND
3	VBAT
4	+12V
5	/Reset



VBAT provides the facility to fit an external battery in conjunction with the onboard battery (1.5V to 3.3V input range) for the backup supply of the 256KB static RAM, Dallas DS1338 56 x 8 serial real time clock, and optional TPM security tamper.

+12V connection defined, but is not required for the VIPER under normal operation. It can be used to supply +12V to the PC/104 stack if required.

A momentary switch (push to make) may be connected across /Reset and GND. Do not connect the switch across /Reset and +5V or +12V.

PL17 – USB client connector

Connector: Neltron 2417SJ-03-F4, 3-way, 2mm Pitch

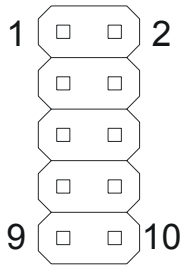
Mating connector: Toby PH200-03H, PH200 Series 2mm housings & crimps

Pin	Signal name
1	USBC-
2	USBC+
3	GND

JP1 – RS485/422 configuration jumpers

Connector: Oupiin 2011-2x5GSB/SN, 10-way, 2.54mm (0.1”) x 2.54mm (0.1”) dual row through-hole unshrouded header

Ref	Pin	Signal name	Pin	Signal name
	1	PL4_RX5-	2	PL4_RX5+
	3	RX5-	4	RX5+
JP1	5	PL4_RX5/TX5-	6	PL4_RX5/TX5+
	7	PL4_RX5+	8	RX5-_120R
	9	PL4_RX5/TX5+	10	RX5/TX5-_120R



JP2 – LCD voltage select jumper

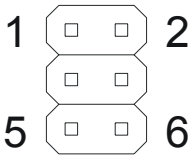
Connector: Oupiin 2011-1x3GSB/SN, 3-way, 2.54mm (0.1”) single row through-hole header

Ref	Pin	Signal name
	1	5V
JP2	2	LCD Logic Supply
	3	3.3V

JP3 – User configuration and reset jumper

Connector: Oupiin 2011-2x3GSB/SN, 6-way, 2.54mm (0.1”) x 2.54mm (0.1”) dual row through-hole unshrouded header

Ref	Pin	Signal name	Pin	Signal name
	1	GND	2	USER_CONFIG1
JP3	3	GND	4	Reserved
	5	GND	6	RESETSW



JP4 – Battery jumper

Connector: Oupiin 2011-1x2GSB/SN, 2-way, 2.54mm (0.1”) single row through-hole header

Ref	Pin	Signal name	Pin	Signal name
JP4	1	Battery Backup Switch Input	2	Battery + Terminal

Status LEDs

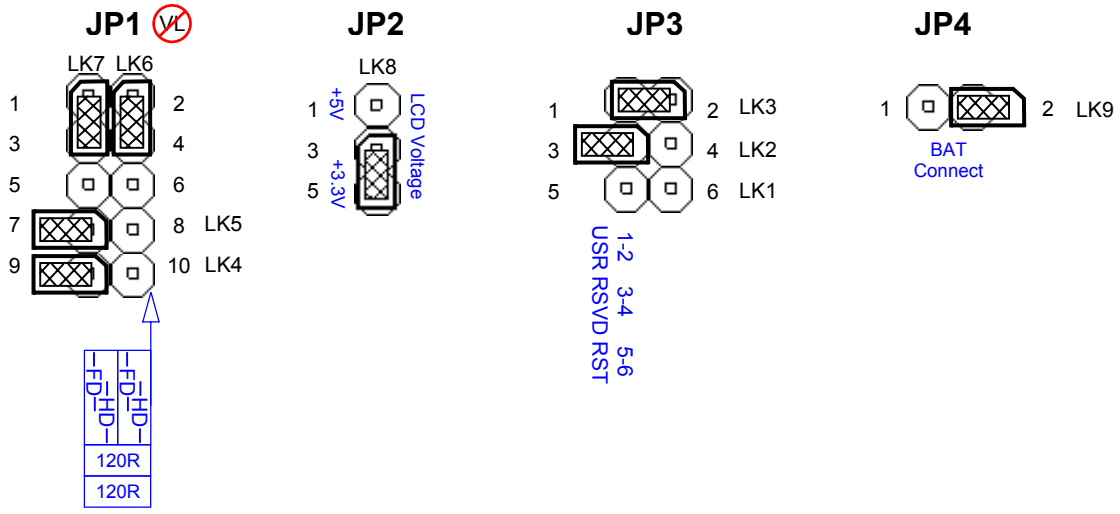
There is a single status LED on the VIPER, which indicates FLASH access to the bootloader FLASH or the main FLASH memory/silicon disk.

Jumpers

There are seven user selectable jumpers on the VIPER. Their use is explained below.

Default settings

The default positions of the jumpers are shown below. Jumper functions described in silkscreen on the board are shown in blue.



Reset – LK1 on JP3

A momentary switch (push to make) may be connected to LK1. When pressed the board goes into a full hardware reset. When the switch is released (open circuit) the board reboots.

Reserved – LK2 on JP3

This jumper is reserved for factory use only. Please do not fit LK2 across JP3 pins 3 and 4.

User configurable jumper 1 – LK3 on JP3

This jumper can be used by an application program to signify a configuration setting.

LK3	Description
	GPIO7 read as ‘0’.
	GPIO7 read as ‘1’.

Default setting: 

The USER_CONFIG1 (GPIO7) signal on LK3 may be used to wake the VIPER from sleep. One way of doing this is to connect a momentary push to make switch to LK3.

RS485/422 configuration – LK4, LK5, LK6, and LK7 on JP1

These jumpers are used to enable/disable the RS485 receive buffer and RS485/422 line termination. See COM5 – RS422/485 interface, page 65, for more details.

LK4	Description
	(RS485 TX/RX) RS422 TX line termination resistor (120Ω) connected.
	(RS485 TX/RX) RS422 TX line termination resistor (120Ω) disconnected.

Default setting: 

LK5	Description
	RS422 RX line termination resistor (120Ω) connected.
	RS422 RX line termination resistor (120Ω) disconnected.

Default setting: 

LK6 & LK7	Description
	RS422 full-duplex.
	RS485 half-duplex.

Default setting: 

 Only fit LK4 and LK5 if the VIPER is at the end of the network.

LCD supply voltage – LK8 on JP2

This jumper selects the supply voltage for the LCD logic supply.

LK8	Description
	Supply LCD logic with 5V.
	Supply LCD logic with 3.3V.

Default setting: 

If the LCD requires a 5V supply, please refer to the LCD datasheet to ensure that the display is compatible with 3.3V logic.

Battery jumper – LK9 on JP4

This jumper connects the battery to the battery back-up circuit.

LK9	Description
	Battery is connected to the board circuit.
	Battery is disconnected from board circuit

Default setting: 

The battery is disconnected when board is shipped. If battery back up is required, jumper LK9 must be fitted to JP4 before installation of the VIPER.

Appendix A – Contacting Arcom

Arcom sales

Arcom's sales team is always available to assist you in choosing the board that best meets your requirements. Contact your local sales office or hotline.

Sales office US

Arcom
7500W 161st Street
Overland Park
Kansas
66085
USA

Tel: 913 549 1000
Fax: 913 549 1002
E-mail: us-sales@arcom.com

Sales office UK

Arcom
Clifton Road
Cambridge
CB1 7EA
UK

Tel: 01223 411 200
Fax: 01223 410 457
E-mail: sales@arcom.co.uk

Comprehensive information about our products is available from our web sites: www.arcom.com and www.arcom.co.uk.

While Arcom's sales team can assist you in making your decision, the final choice of boards or systems is solely and wholly the responsibility of the buyer. Arcom's entire liability in respect of the boards or systems is as set out in Arcom's standard terms and conditions of sale. If you intend to write your own low level software, you can start with the source code on the disk supplied. This is example code only to illustrate use on Arcom's products. It has not been commercially tested. No warranty is made in respect of this code and Arcom shall incur no liability whatsoever or howsoever arising from any use made of the code.

Technical support

Arcom has a team of technical support engineers available to provide a quick *and free* response to your technical queries.

Technical support US

Tel: 913 549 1010
Fax: 913 549 1001
E-mail: us-support@arcom.com

Technical support UK

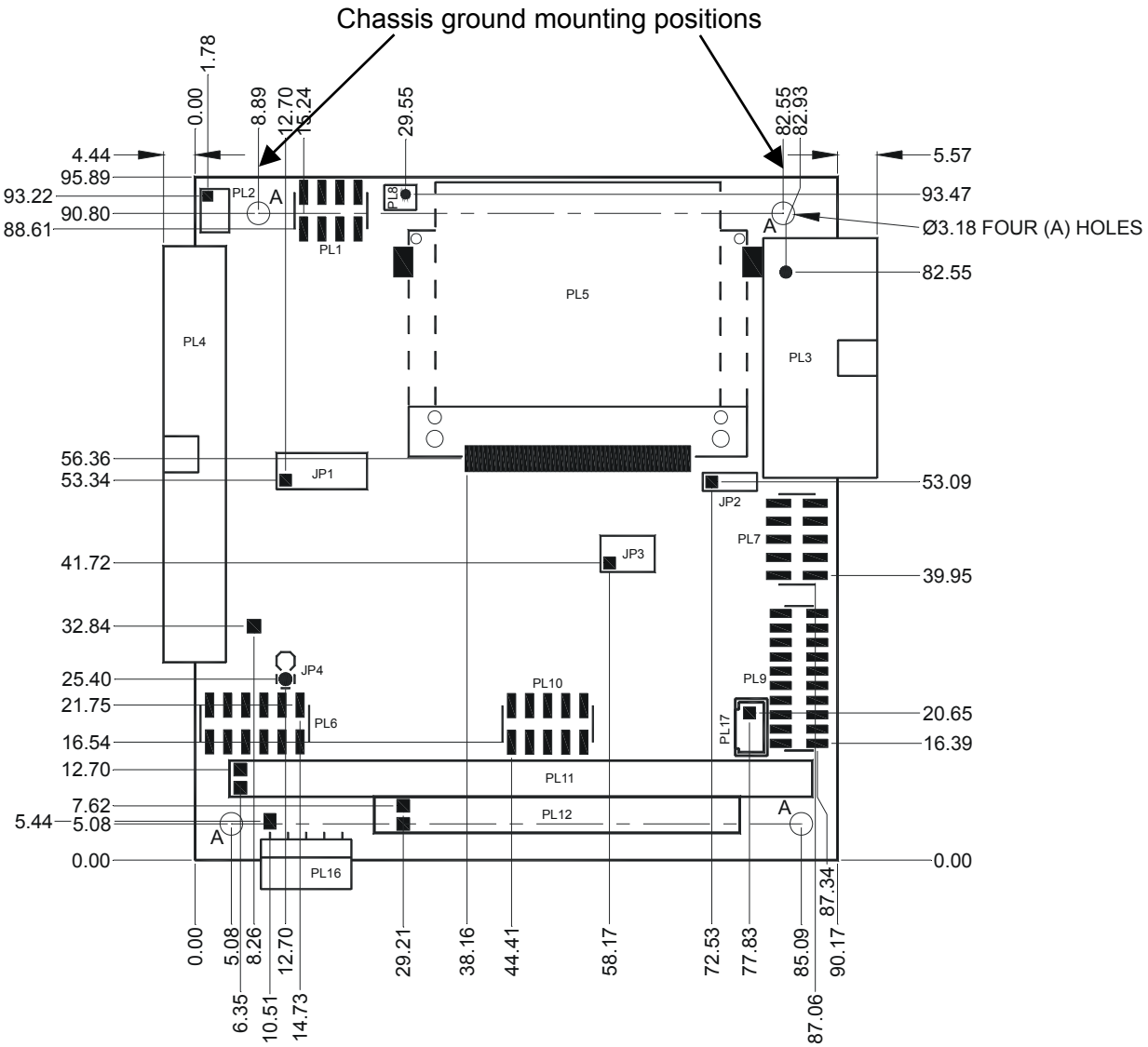
Tel: +44 (0)1223 412 428
Fax: +44 (0)1223 403 409
E-mail: euro-support@arcom.com

Appendix B – Specification

Microprocessor	400MHz (VIPER) or 200MHz (VIPER-Lite) PXA255 processor.	
Memory	16MB, 64MB 3.3V un-buffered SDRAM. 16MB, 32MB Intel StrataFLASH. 1MB Bootloader ROM. VL 256k SRAM (battery backed).	
Graphics controller	PXA255 Flat panel controller offering resolutions: • 320 x 240, 8/16 bpp. • 640 x 480, 8/16 bpp. • 800 x 600, 8 bpp (not recommended by Arcom).	
Peripherals	Serial:	RS232 on COM1, COM2, COM3, & COM4 VL RS422/485 on COM5. VL
	CompactFLASH:	One Type I/II CompactFLASH socket.
	VL Audio:	16-bit AC'97-compliant CODEC, stereo. 20Hz to 20kHz In / Out frequency response
	VL USB Host:	Dual channel v1.1 host support
	USB Client	One channel v1.1 client support
	Network:	One 10/100BaseTX NIC port
	VL TPM (Optional):	TCG/TCPA V1.1b Compatibility 1024-bit RSA signature in 100 ms.
Temperature	Operating:	-20°C (-4°F) to +70°C (+158°F) (commercial). -40°C (-40°F) to +85°C (+185°F) (industrial).
Humidity	10% to 90% RH (non-condensing).	
Real time clock	Accuracy +/- 1 minute/month.	
Software	RedBoot Bootloader for embedded Linux or VxWorks. Eboot Bootloader for Windows CE.	
Power requirement	5V +/- 5%. 2W typical consumption (no LCD, CF, or USB devices fitted). 49mA (245mW) in sleep mode.	
Battery input	1.5v to 3.3v, typical discharge 2μA.	
Dimensions	PC/104 compatible format: 3.775" x 3.550", 96mm x 91mm.	
Weight	99 grams.	

Appendix C – Mechanical diagram

Unit of measure = mm (1inch = 25.4mm)



NOTES
1) ALL CONNECTOR DIMENSIONS ARE TAKEN FROM PIN 1

When mounting the VIPER use only M3 (metric) or 4-40 (imperial) screws. The mounting pad is 6.35mm, 0.25” and the hole is 3.175mm, 0.125”, so ensure any washers fitted are smaller than the pad.

Using oversized screws and washers, or tooth locking washers, can cause short circuits and over-voltage conditions.

We recommend that you use a Loctite screw thread lock or a similar product over tooth locking washers.

Appendix D – Reference information

Product information

Product notices, updated drivers, support material, 24hr-online ordering:

www.arcom.com

PC/104 Consortium

PC/104 specifications, vendor information and available add on products:

www.PC/104.org

USB Information

Universal Serial Bus (USB) specification and product information:

www.usb.org

CFA (CompactFlash Association)

CF+ and CompactFlash specification and product information:

www.compactflash.org

TCG (Trusted Computing Group)

TCG TPM specification:

https://www.trustedcomputinggroup.org/home

Intel

Intel XScale™ PXA255 processor documentation:

www.intel.com

www.intel.com/design/pca/prodbref/252780.htm

Standard Microsystems Corporation

SMSC SMC91C111 Ethernet controller documentation:

www.smsc.com

Exar Corporation

Exar XR16C2850 DUART with 128Byte FIFO documentation:

www.exar.com

National Semiconductor Corporation

National Semiconductor LM4549 AC'97 Codec documentation:

www.national.com

Koninklijke Philips Electronics N.V.

Philips ISP1160 USB host controller documentation:

www.philips.com

Maxim Integrated Products Inc.

Maxim DS1338 56 x 8 serial real time clock documentation:

www.maxim-ic.com

Linear Technology Corporation

Linear Technology LTC1659 Micropower DAC documentation:

www.linear.com

Appendix E – Acronyms and abbreviations

Amp	Amplifier
ATA	Advanced Technology Attachment
BTUART	Bluetooth Universal Asynchronous Receiver / Transmitter
CAN	Control Area Network
CCCR	Core Clock Configuration Register
CF	Compact Flash
CFI	Common FLASH Interface
CODEC	Coder/Decoder
COM	Communication Port
CPLD	Complex Programmable Logic Device
CPU	Central Processing Unit (PXA255)
CMOS	Complementary Metal Oxide Semiconductor
CRT	Cathode Ray Tube
DAC	Digital to Analog Converter
DMA	Direct Memory Access
DUART	Dual Universal Asynchronous Receiver / Transmitter
EEPROM	Electrically Erasable and Programmable Read-Only Memory
EMC	Electromagnetic Compatibility
EPROM	Erasable and Programmable Read-Only Memory
EXT2	Linux's standard file system type
FFUART	Full Function Universal Asynchronous Receiver / Transmitter
FIFO	First-In First-Out
FLASH	A non-volatile memory that is preserved even if the power is lost
FPIF1	Flat Panel Interface
GPIO	General Purpose Input/Output
I2C	(=IIC) Intra Integrated Circuit bus
ICE	In-Circuit-Emulator
ICR	Interrupt Control and Reset register
IEEE	Institute of Electrical and Electronics Engineers
IO	Input/Output
ISA	Industry Standard Architecture, Bus in the IBM-PC
JTAG	Joint Test Action Group of IEEE
LED	Light Emitting Diode
LCD	Liquid Crystal Display
LSB	Least Significant Bit
LVDS	Low Voltage Differential Signaling
NA	Not Applicable
NC	No Connect
NU	Not Used
OS	Operating System
PC/104	Offers full architecture, hardware, and software compatibility with the PC ISA bus, but in ultra-compact 96mm x 91mm (3.775" x 3.550") stackable modules
PCB	Printed Circuit Board

PROM	Programmable Read-Only Memory
PWM	Pulse-Width Modulation
RAM	Random Access Memory
Reg	Regulator
RSA	public key cryptosystem invented by Rivest, Shamir, and Adleman
RTC	Real Time Clock
RX	Receive
SBC	Single Board Computer
SDRAM	Synchronous Dynamic Random Access Memory
SRAM	Static Random Access Memory
STN	Super Twisted Nematic, technology of passive matrix liquid crystal
STUART	Standard Universal Asynchronous Receiver / Transmitter
TCG/TCPA	Trusted Computing Group / Platform Alliance
TPM	Trusted Platform Module
TFT	Thin Film Transistor, a type of LCD flat-panel display screen
TX	Transmit
UART	Universal Asynchronous Receiver / Transmitter
UPS	Uninterruptible Power Supply
USB	Universal Serial Bus
VAC	Voltage Alternating Current
VDC	Voltage Direct Current
VGA	Video Graphics Adapter, display resolution 640 x 480 pixels
VIPER-ICE	VIPER-Industrial Compact Enclosure

Appendix F – RoHS-6 Compliance - Materials Declaration Form

Arcom
A MEMBER OF EUROTECH GROUP

Confirmation of Environmental Compatibility for Supplied Products

Substance	Maximum concentration
Lead	0.1% by weight in homogeneous materials
Mercury	0.1% by weight in homogeneous materials
Hexavalent chromium	0.1% by weight in homogeneous materials
Polybrominated biphenyls (PBBs)	0.1% by weight in homogeneous materials
Polybrominated diphenyl ethers (PBDEs)	0.1% by weight in homogeneous materials
Cadmium	0.01% by weight in homogeneous materials

The products covered by this certificate include:

Product Name	Arcom Part Number
VIPER	VIPER-M64-F32-V2-R6
VIPER	VIPER-M64-F16-V2-R6
VIPER	VIPER-M64-F32-V2-I-R6
VIPER	VIPER-M64-F16-V2-I-R6
VIPER-Lite	VIPERL-M64-F32-R6
VIPER-Lite	VIPERL-M64-F16-R6

Arcom has based its material content knowledge on a combination of information provided by third parties and auditing our suppliers and sub-contractor's operational activities and arrangements. This information is archived within the associated Technical Construction File. Arcom has taken reasonable steps to provide representative and accurate information, though may not have conducted destructive testing or chemical analysis on incoming components and materials.

Additionally, packaging used by Arcom for its products complies with the EU Directive 2004/12/EC in that the total concentration of the heavy metals cadmium, hexavalent chromium, lead and mercury do not exceed 100 ppm.

Index

A

active display signal · 36
address map · 19
amplifier · 5, 7, 16, 56
anti-static · 12
assignments, GPIO pins · 22
audio · 5, 7, 16, 56
  connector · 91
  power management · 84

B

backlight · 7
  brightness · 37
  enable · 37
  inverter connector · 42
base TX ethernet · 62
battery · 73
battery input · 5, 6
block diagram · 18
board · 4
  custom configurations · 4
bootloader · 7, 16
breakout board · 62
bus, expansion · 17

C

cache · 7
clock · 8, 21, 26, 102
CODEC · 7
COM · 5
  ports connector · 89
COM1 · 64
COM2 · 64
COM3 · 64
COM4 · 65
COM5 · 65, 99
CompactFLASH · 5, 6, 7, 15, 28
  connector · 90
  power · 83
connector · 85, 86
  audio · 91
  CompactFLASH · 90
  COMS port · 89
  ethernet · 87
  ethernet status · 87
  JTAG · 93
  LCD · 88
  PC/104 · 94
  power · 95
  USB · 91
contact details · 101
controller, graphics · 102
custom configurations · 4

D

dark boot · 98
development kits · 10, 11
digital I/O · 5, 6
dimensions · 102
display · 34

E

EMC · 12
EPROM · 7
ethernet · 5, 6, 8, 16, 62
  breakout board · 62
  connector · 87
  LED · 5, 6
  power management · 83
expansion bus · 17
external device power · 78
external interrupt · 30

F

features · 7
FIFO · 7
flash access LED · 85
FLASH memory · 27
flat panel · 34
FPIF · 38, 43, 48, 53

G

general purpose I/O · 57
GPIO · 8
  pins assignments · 22
GPIO connector · 92
graphics controller · 102

H

heat sink · 21
humidity · 102

I

I/O · 5, 6
Intel PXA255 · 4
interface, USB · 60
internal interrupt · 30
interrupt · 30
  external · 30
  internal · 30

J

JTAG · 5, 6, 8
  connector · 93
jumper · 5, 6, 8, 13, 85, 98
  header · 96

L

LAN · 16
LCD · 34, 38, 48, 53
  backlight brightness · 37
  backlight enable · 37
  connector · 88
  generic connector · 40, 46, 51
  logic supply enable · 37
  SBC cable connector · 39, 45, 50, 54
LED · 5, 6, 85, 97
Linux · 15, 16, 21, 27, 29, 31, 32, 82, 102
  PC/104 interrupts · 32
LK1 · 85, 86, 96, 98
LK2 · 98
LK3 · 98
LK4 · 99, 100
LK5 · 99, 100
LK6 · 99, 100
LK7 · 99, 100

M

map, address · 19
mechanical diagram · 103
memory · 7, 27, 102
microphone · 5, 7, 16, 56
microprocessor · 102
MMU · 20

N

network · 8

O

on board device power · 77
operating frequency · 21

P

passive display signal · 36
PC/104 · 30, 67
  consortium · 104
  interface · 5
PC/104 interrupts
  Linux · 32
  Windows CE · 33
peripheral · 102
peripheral control module · 21
PL1 · 85, 86, 87
PL10 · 85, 86, 93
PL11 · 85, 86, 94
PL12 · 85, 86, 94
PL13 · 86
PL16 · 85, 86, 95
PL17 · 85, 86, 96
PL2 · 85, 86, 87
PL3 · 85, 86, 88
PL4 · 85, 86, 89
PL5 · 85, 86, 90
PL6 · 85, 86, 91
PL7 · 85, 86, 91
PL8 · 85, 86, 92
PL9 · 85, 86, 92
port
  serial · 7, 64
  USB · 7
power · 5, 6, 8, 73, 102
  audio · 84
  CompactFLASH · 83
  connector · 73, 95
  ethernet · 83
  external device · 78
  management · 74
  processor · 75, 81
  supply · 73
  UART · 83
  USB · 83
  voltage · 73
processor · 4, 5, 6, 7, 102
  power · 75
  power management · 81
  PXA255 · 21
product information · 104
PXA255 · 21

R

RAM, static · 28
real time clock · 8, 26, 102
RedBoot · 102
reset · 98
resolution · 7
RoHS compliance · 12

RS232 · 7, 15, 64, 65
RS422 · 7, 15, 65, 99, 100
RS485 · 7, 15, 65, 99, 100
RTC · 8, 26

S

SDRAM · 27
serial port · 5, 6, 7, 15, 64
silicon disk · 7, 27
software · 102
source code · 101
specification · 102
SRAM · 7
static · 12
static RAM · 28
status LED · 97
STN · 5, 6, 36, 38, 48, 53
  bias connector · 42
StrataFLASH · 5, 6, 7, 27
support products · 9
support, technical · 101
system
  control module · 21
  memory · 7

T

technical support · 101
temperature · 102
TFT · 5, 6, 7, 9, 35, 38, 43, 48
timer, watchdog · 26
TPM · 71, 84
TPM Tamper detect connector · 92
trusted platform module · 71, 84

U

UART · 7
  power management · 83
USB · 5, 6, 7, 16, 104
  connector · 91
  interface · 60
  power management · 83

V

video · 7
VIPER · 4
  custom configurations · 4
  development kits · 11
  features · 7
  support products · 9
  using · 15
VIPER-ICE development kits · 10
VIPER-Lite · 4
  custom configurations · 4
  development kits · 11
  features · 7
  features not available · 4, 13, 18
  support products · 9
  using · 15
VxWorks · 15, 16, 21, 27, 102

W

wake up events · 84
watchdog · 8
  timer · 26
weight · 102
Windows CE · 15, 16, 21, 27, 102
  PC/104 · 33